

Fig. 1
Prior Art

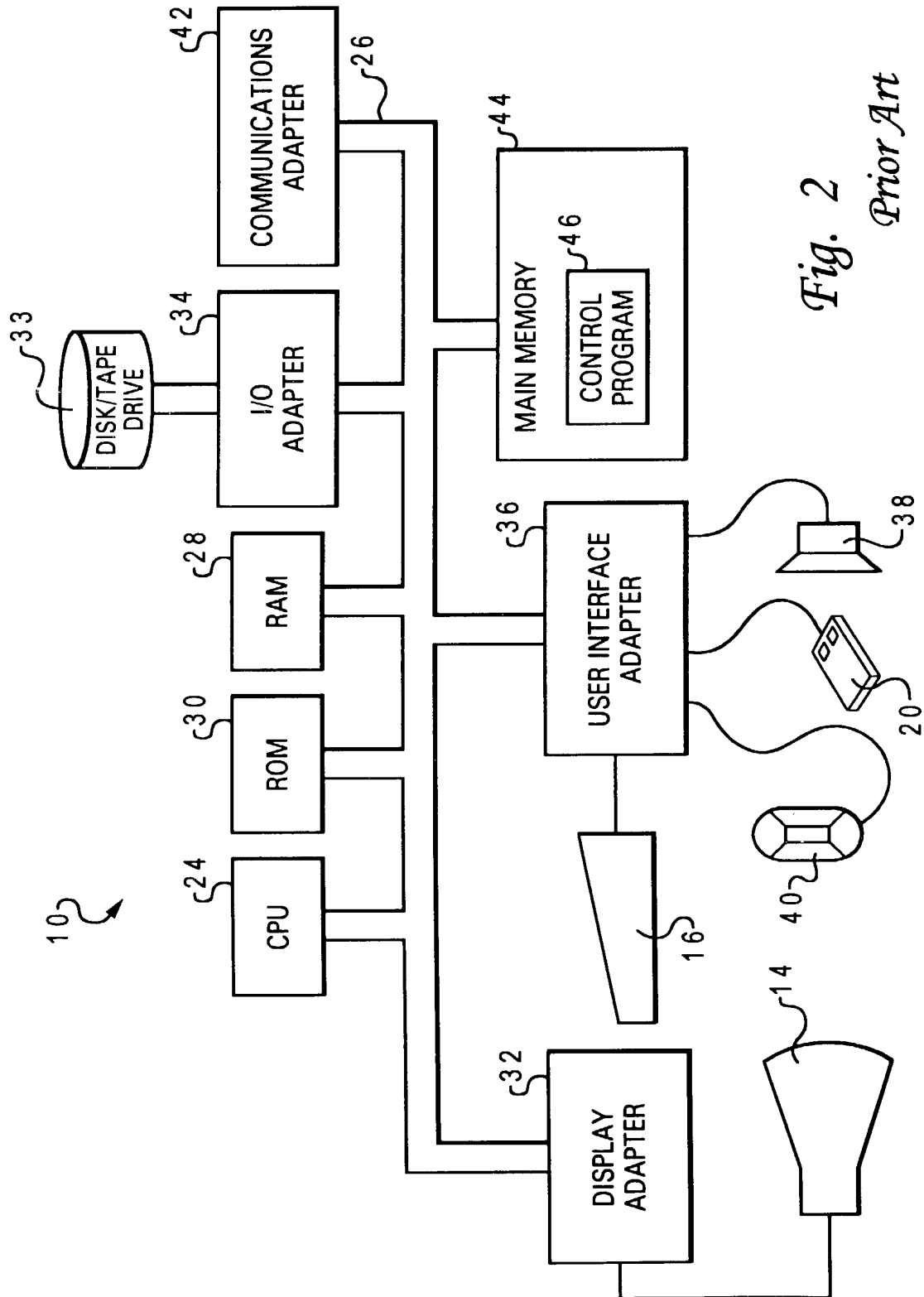


Fig. 2
Prior Art

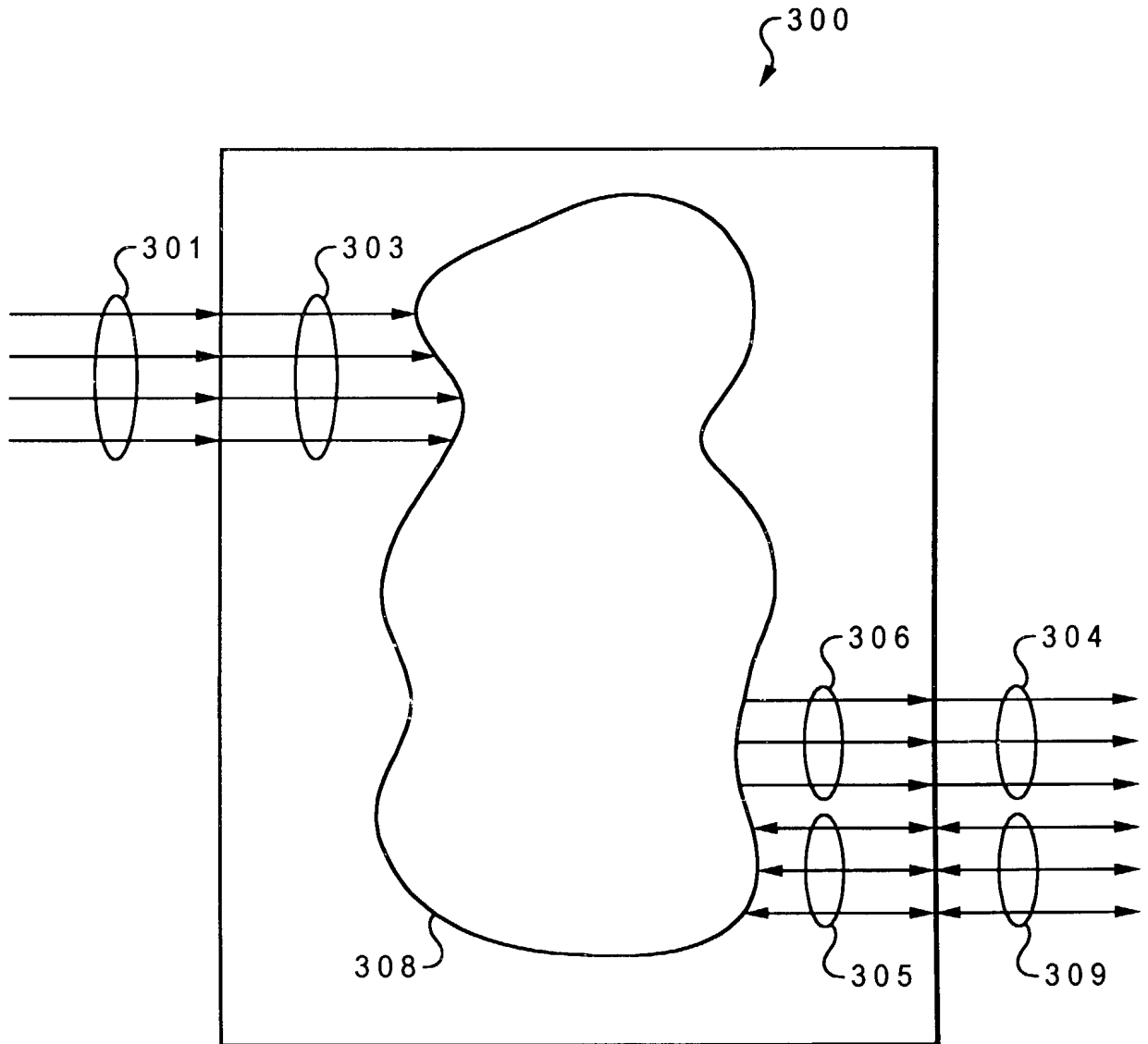
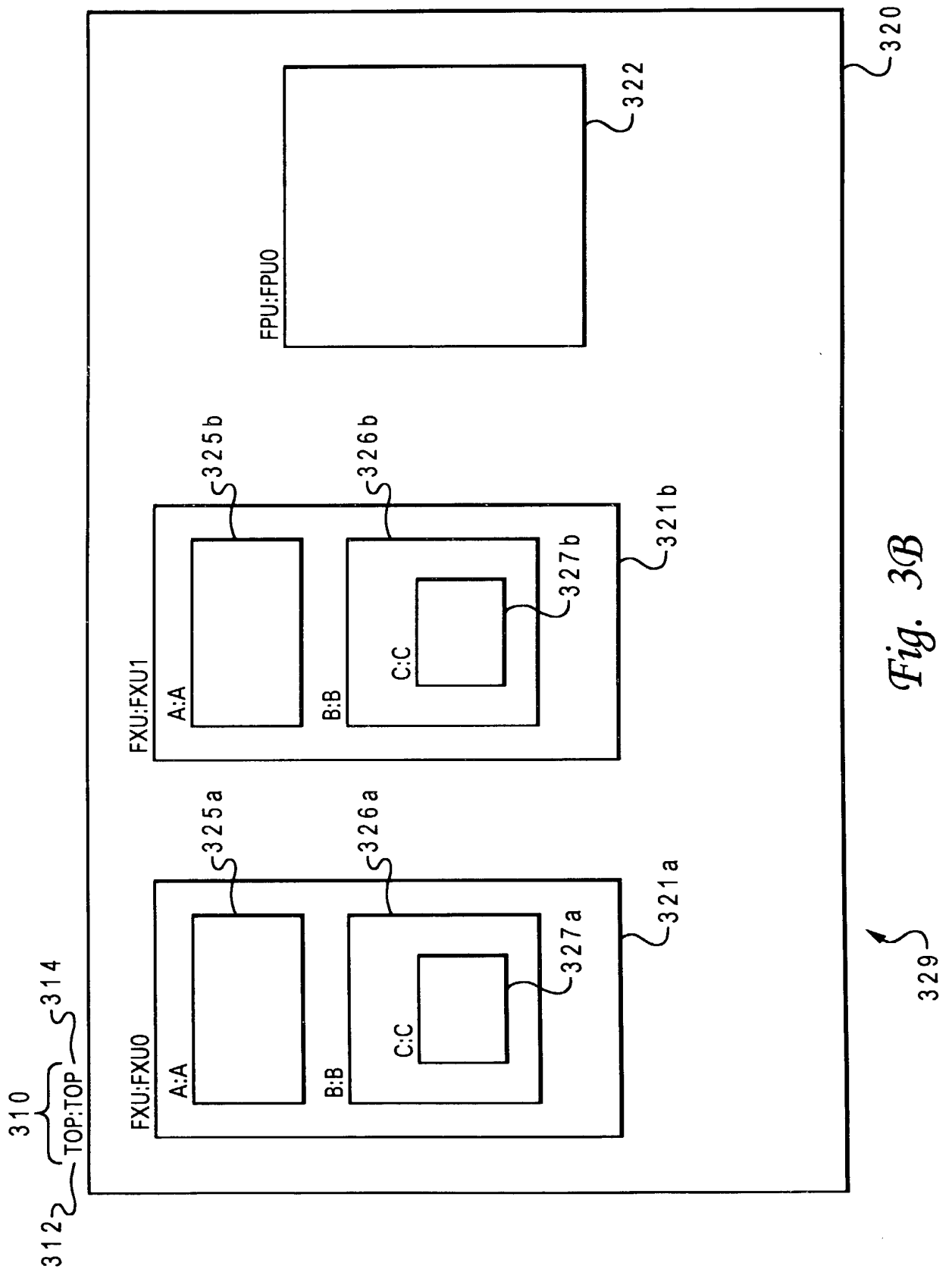


Fig. 3A



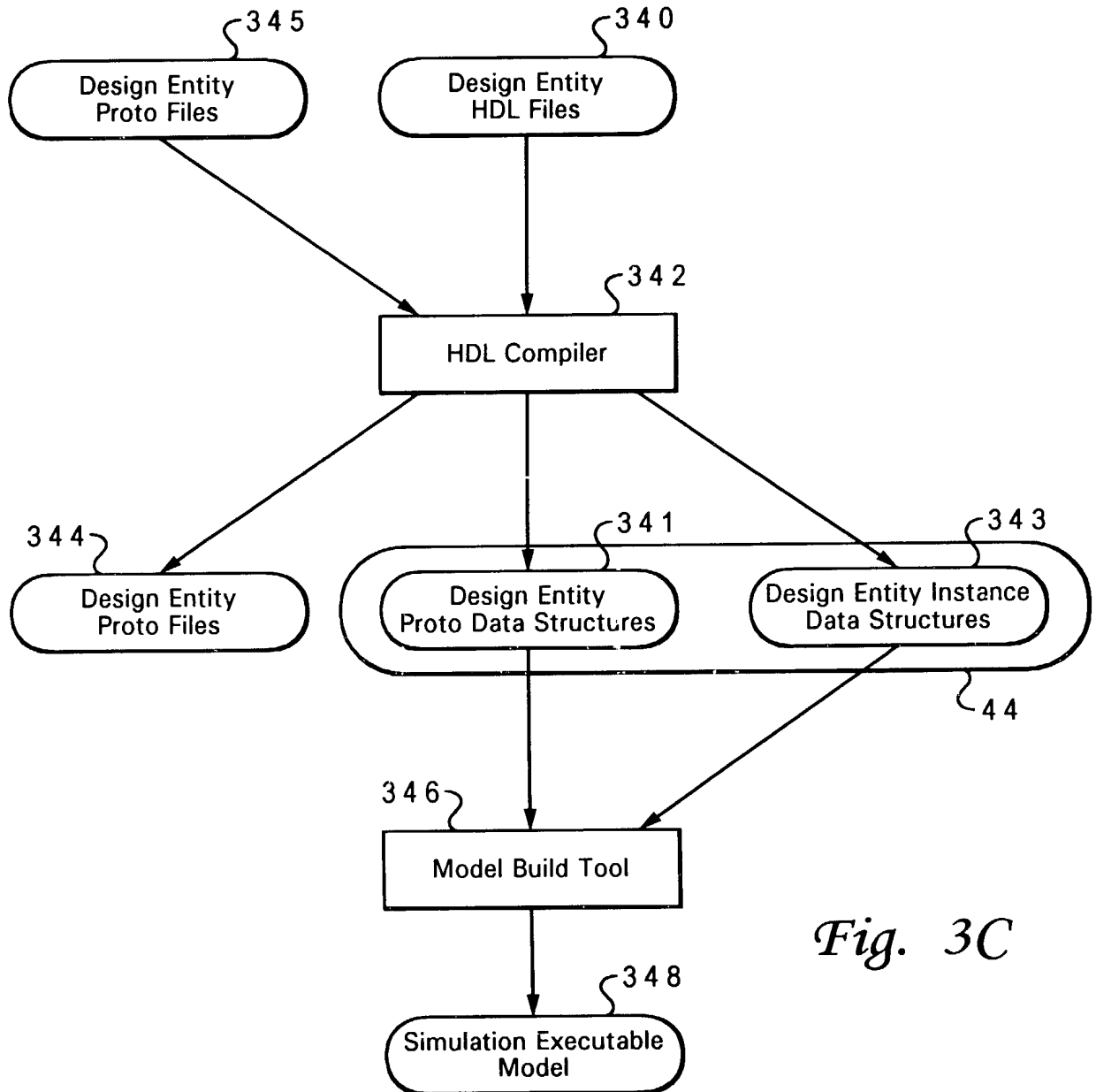


Fig. 3C

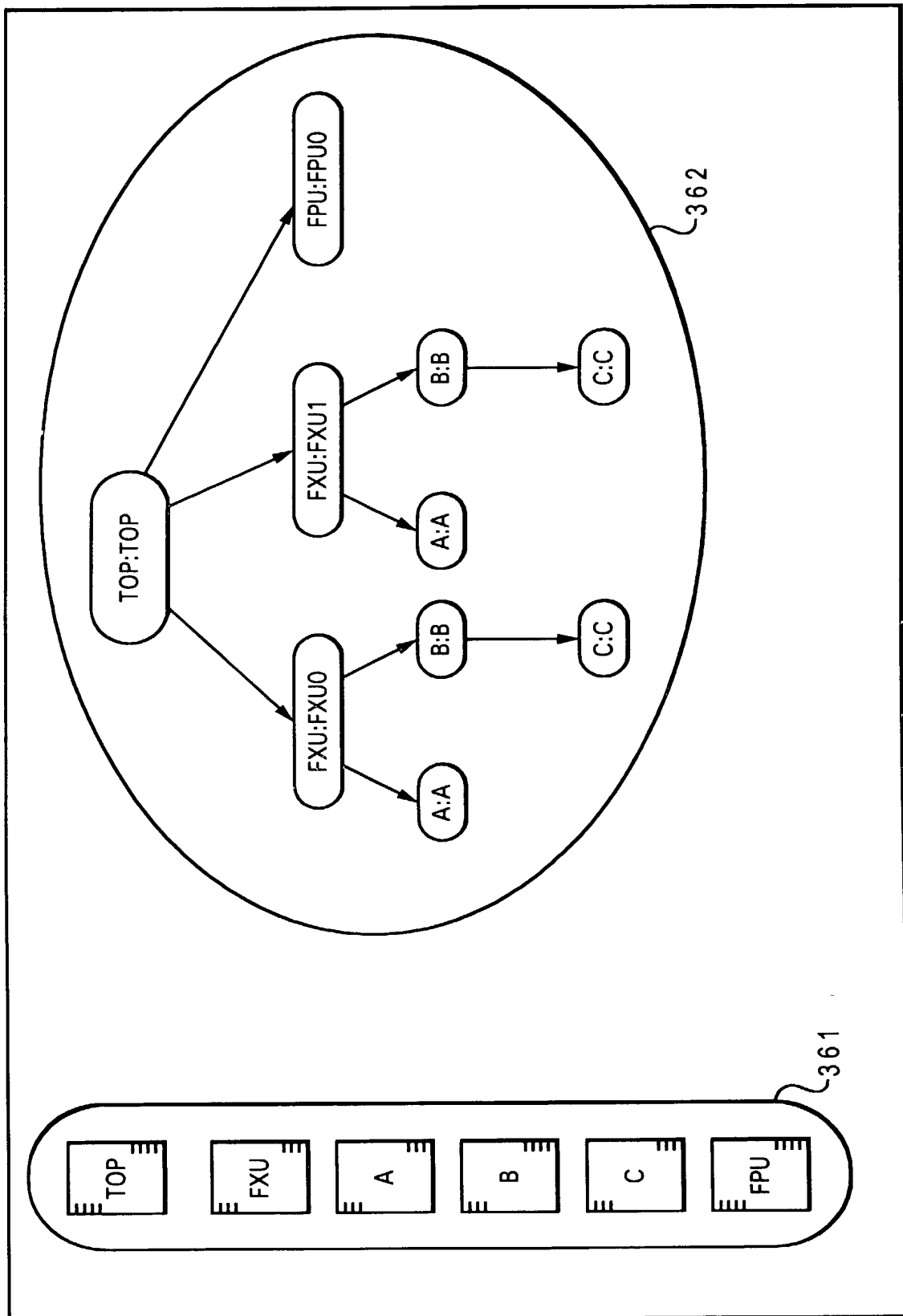


Fig. 3D

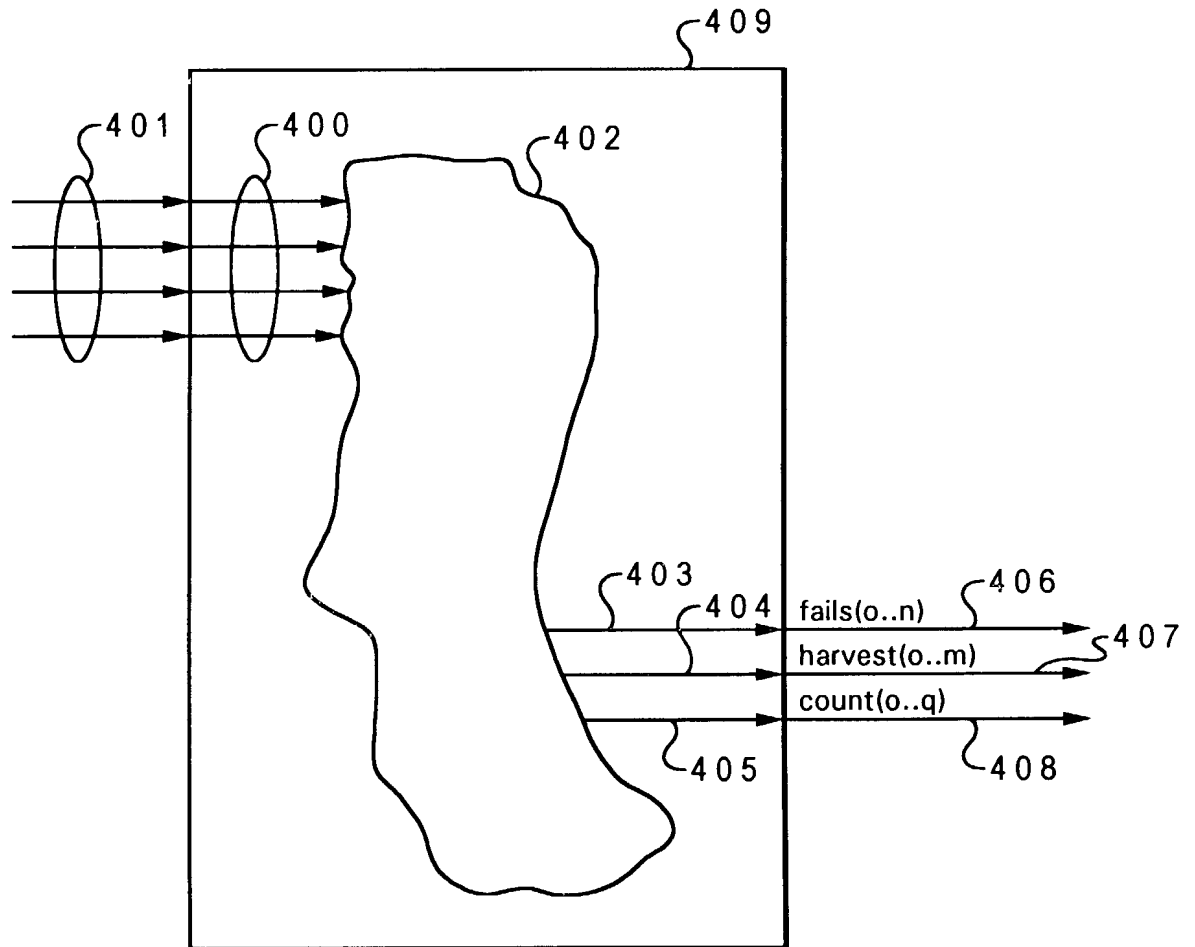


Fig. 4A

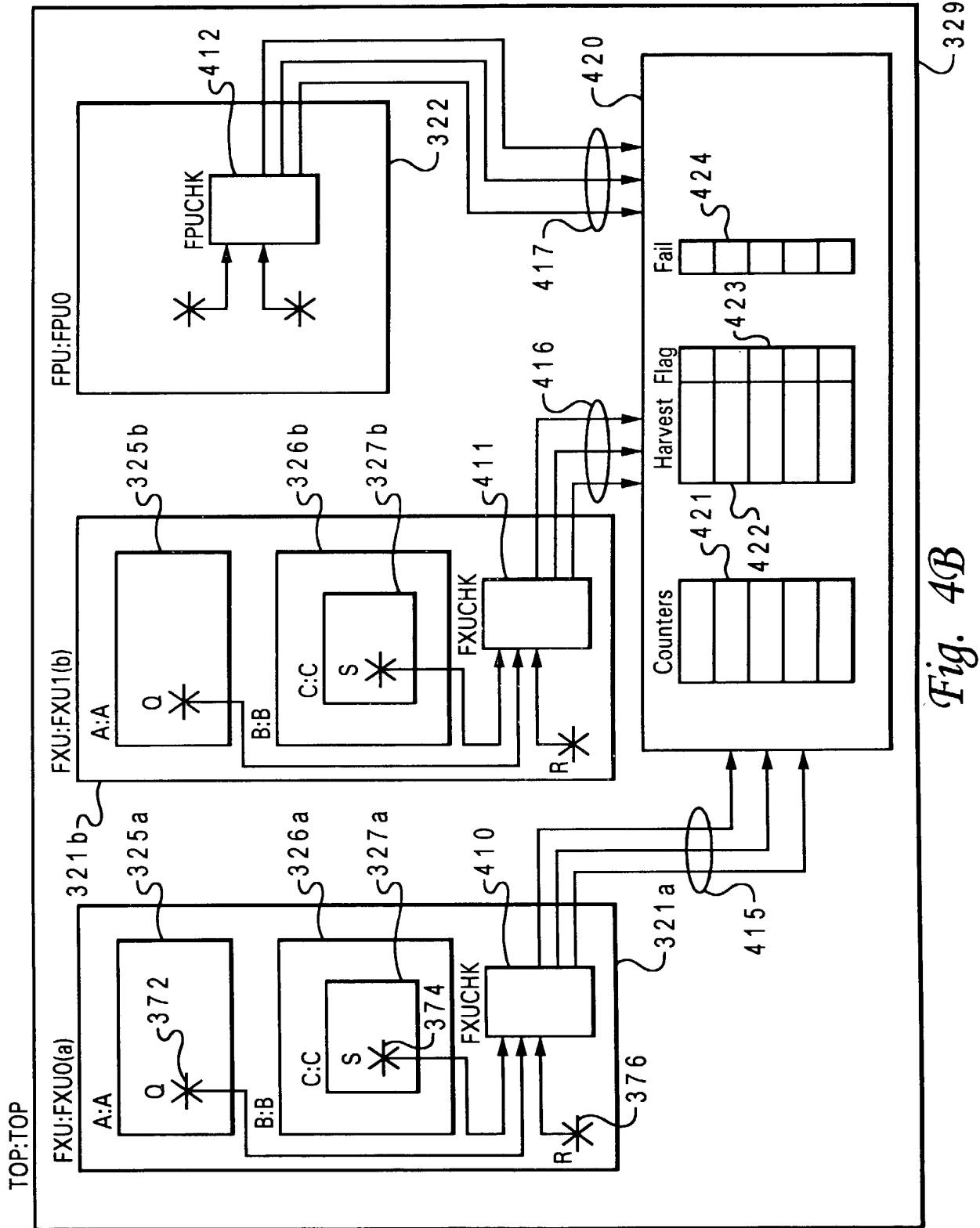


Fig. 4B

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ENTITY FXUCHK IS

```

PORT(  S_IN      :  IN std_ulogic;
        Q_IN      :  IN std_ulogic;
        R_IN      :  IN std_ulogic;
        clock     :  IN std_ulogic;
        fails     :  OUT std_ulogic_vector(0 to 1);
        counts    :  OUT std_ulogic_vector(0 to 2);
        harvests  :  OUT std_ulogic_vector(0 to 1);
);

```

4 5 0

```

4 5 2 { --!! BEGIN
      --!! Design Entity: FXU;

```

```

4 5 3 { --!! Inputs
      --!! S_IN      =>  B.C.S;
      --!! Q_IN      =>  A.Q;
      --!! R_IN      =>  R;
      --!! CLOCK     =>  clock;
      --!! End Inputs

```

```

4 5 4 { --!! Fail Outputs;
      --!! 0 : "Fail message for failure event 0";
      --!! 1 : "Fail message for failure event 1";
      --!! End Fail Outputs;

```

```

4 5 5 { --!! Count Outputs;
      --!! 0 : <event0> clock;
      --!! 1 : <event1> clock;
      --!! 2 : <event2> clock;
      --!! End Count Outputs;

```

```

4 5 6 { --!! Harvest Outputs;
      --!! 0 : "Message for harvest event 0";
      --!! 1 : "Message for harvest event 1";
      --!! End Harvest Outputs;

```

```

4 5 7 { --!! End;

```

4 5 1

4 4 0

ARCHITECTURE example of FXUCHK IS

BEGIN

... HDL code for entity body section ...

END;

4 5 8

Fig. 4C

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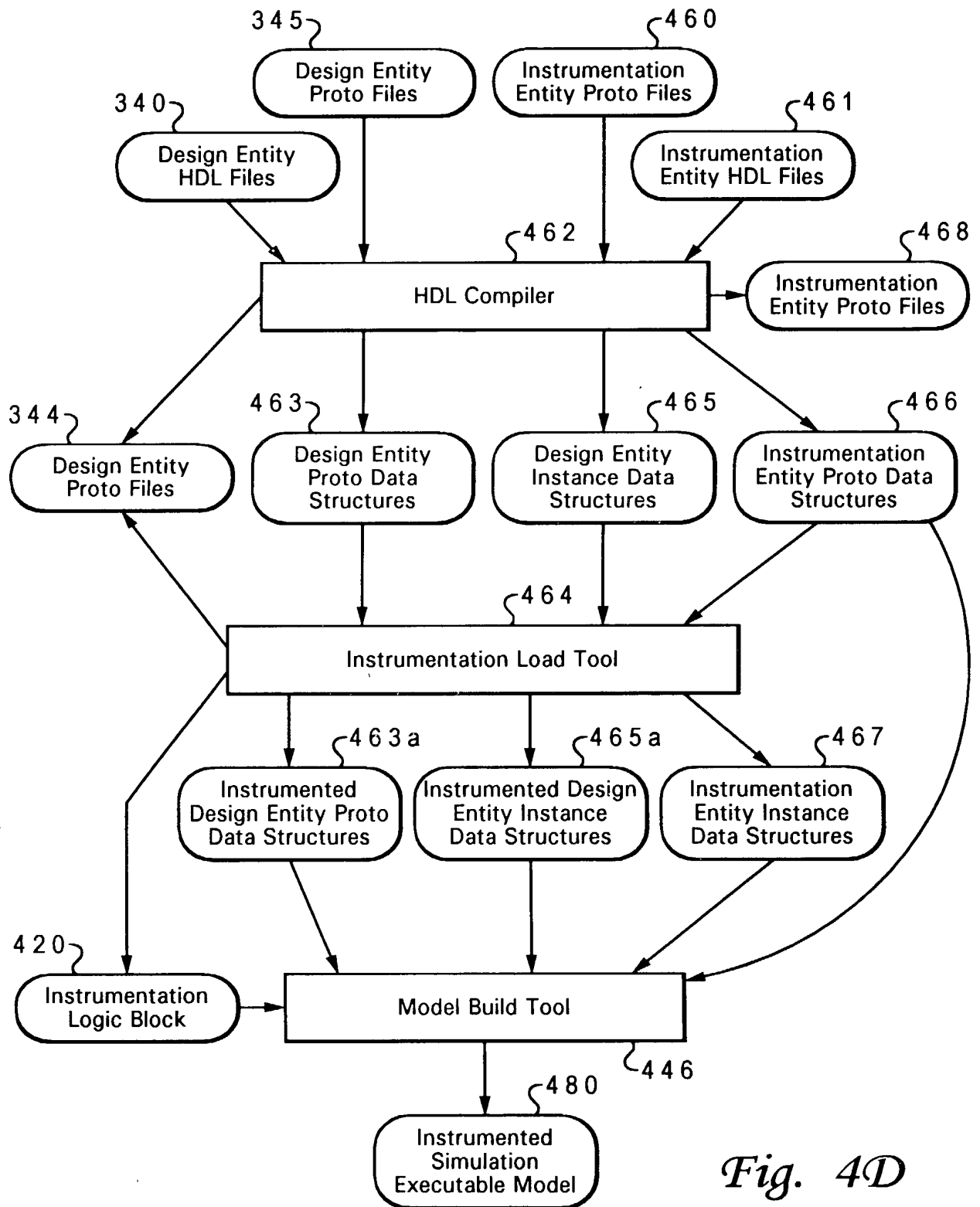


Fig. 4D

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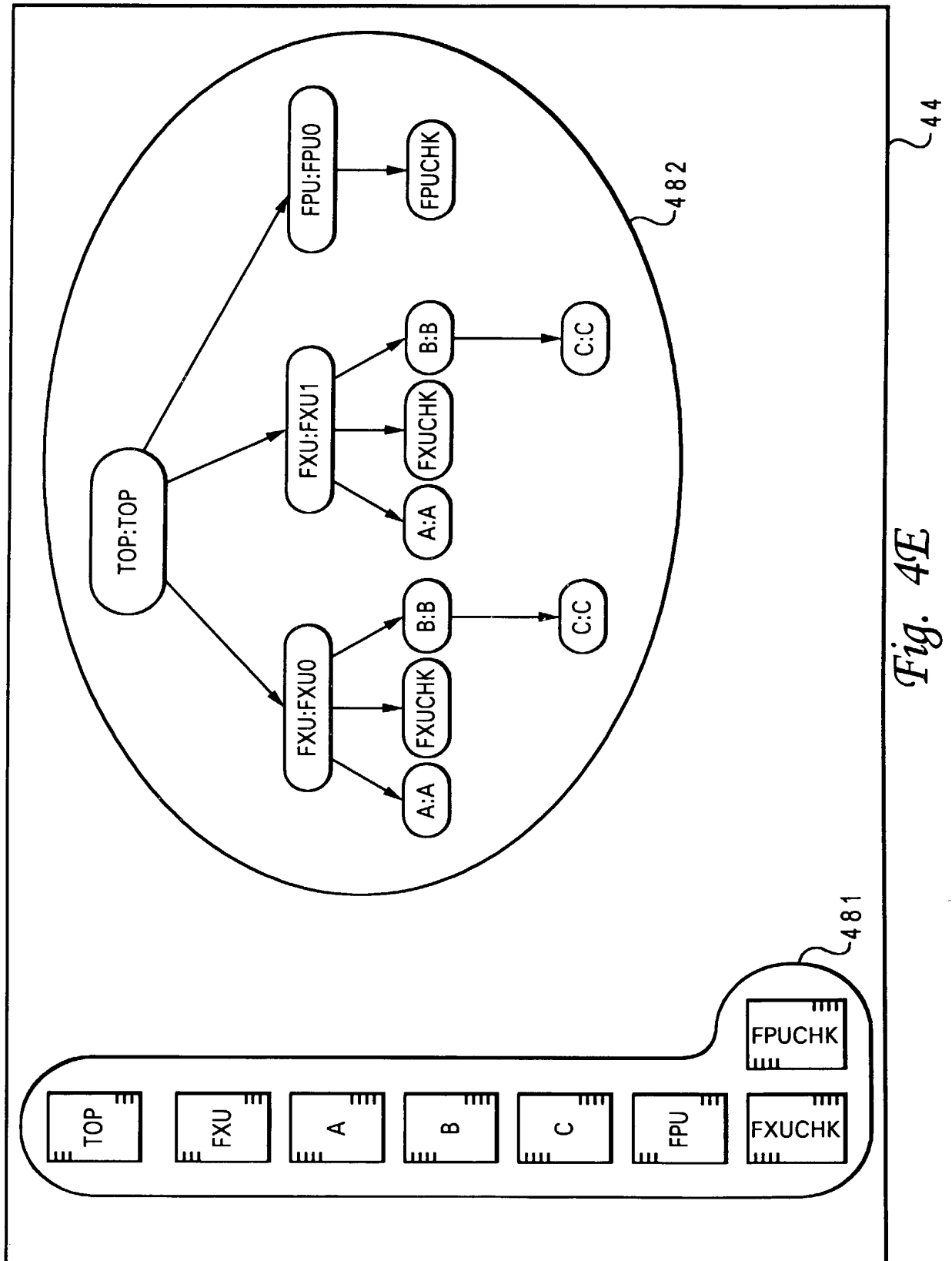
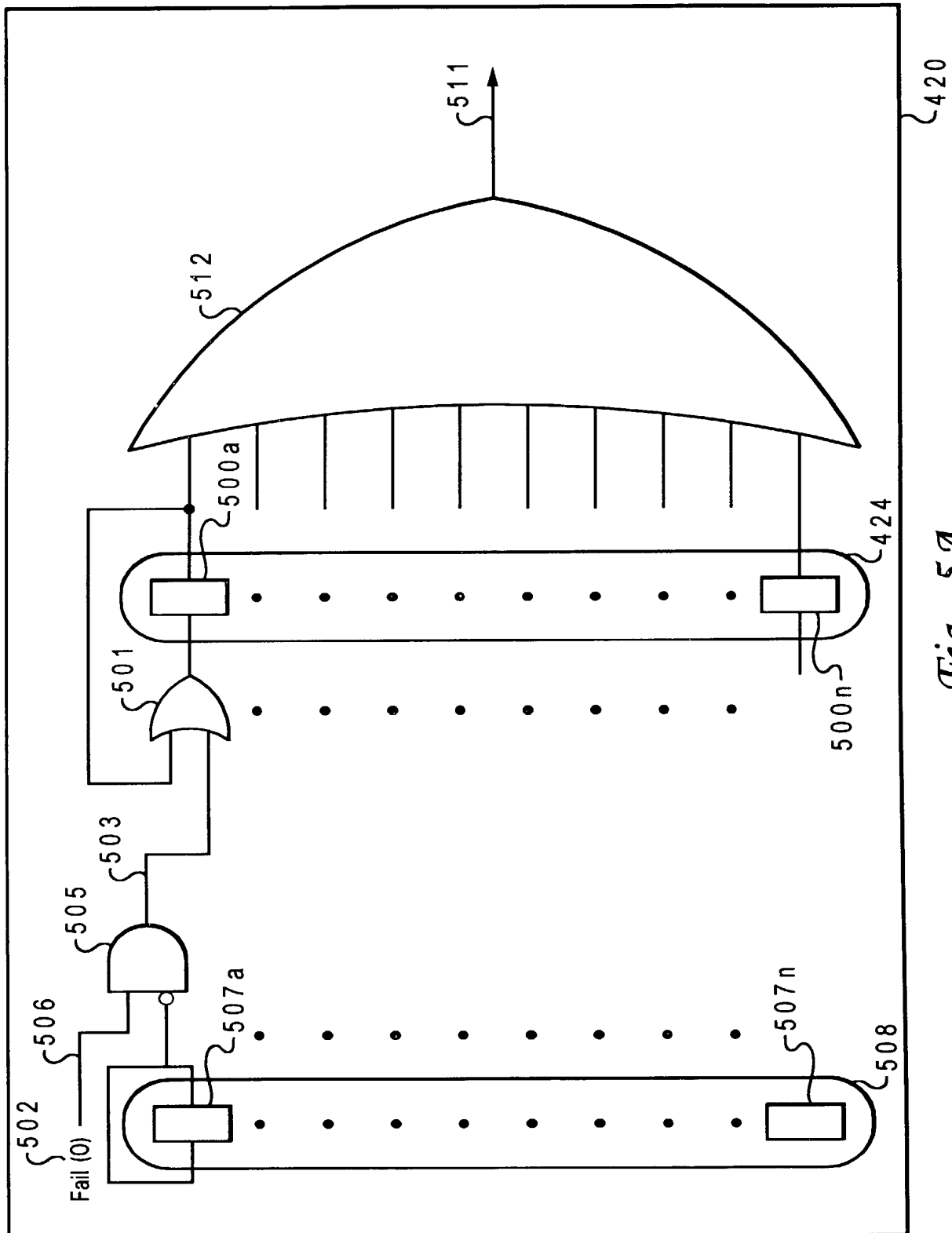


Fig. 4E

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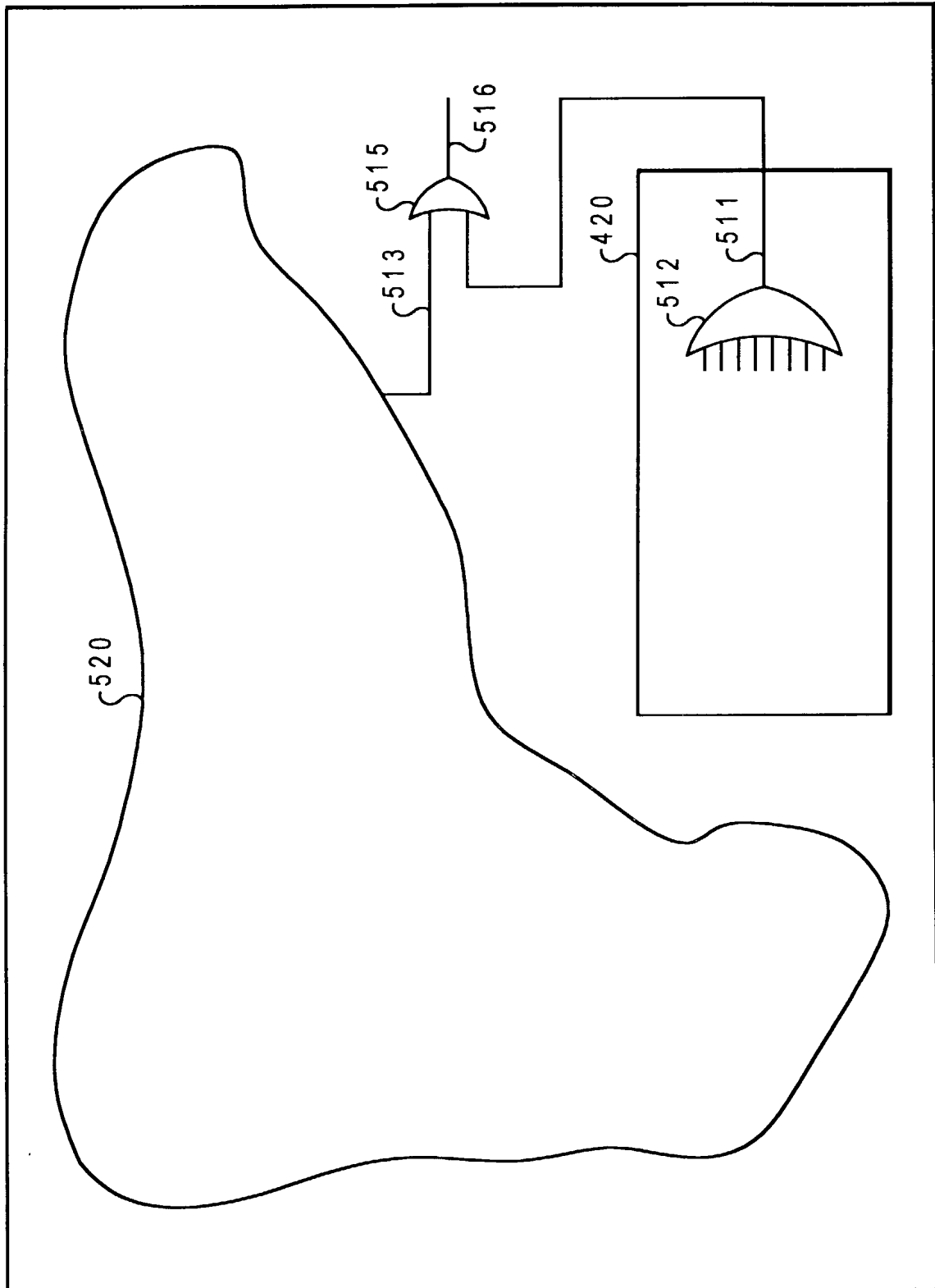


Fig. 5B

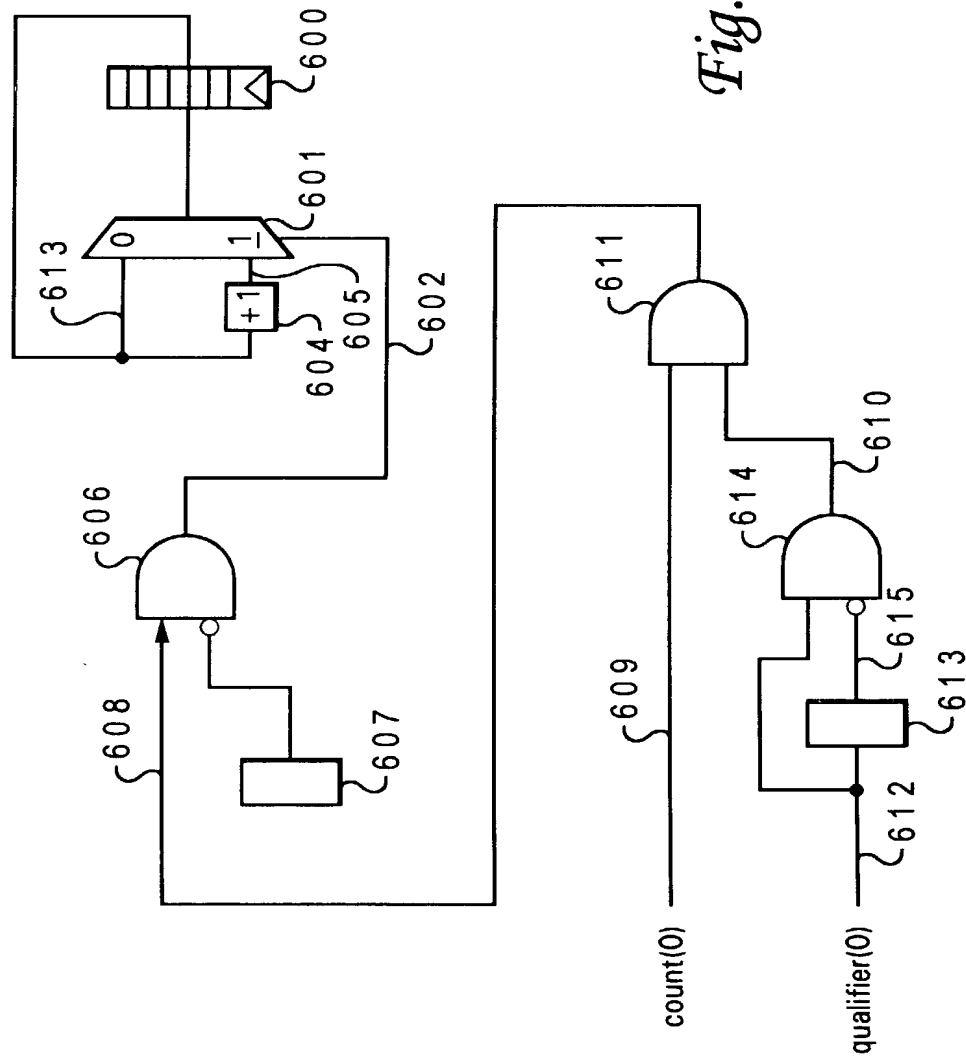


Fig. 6A

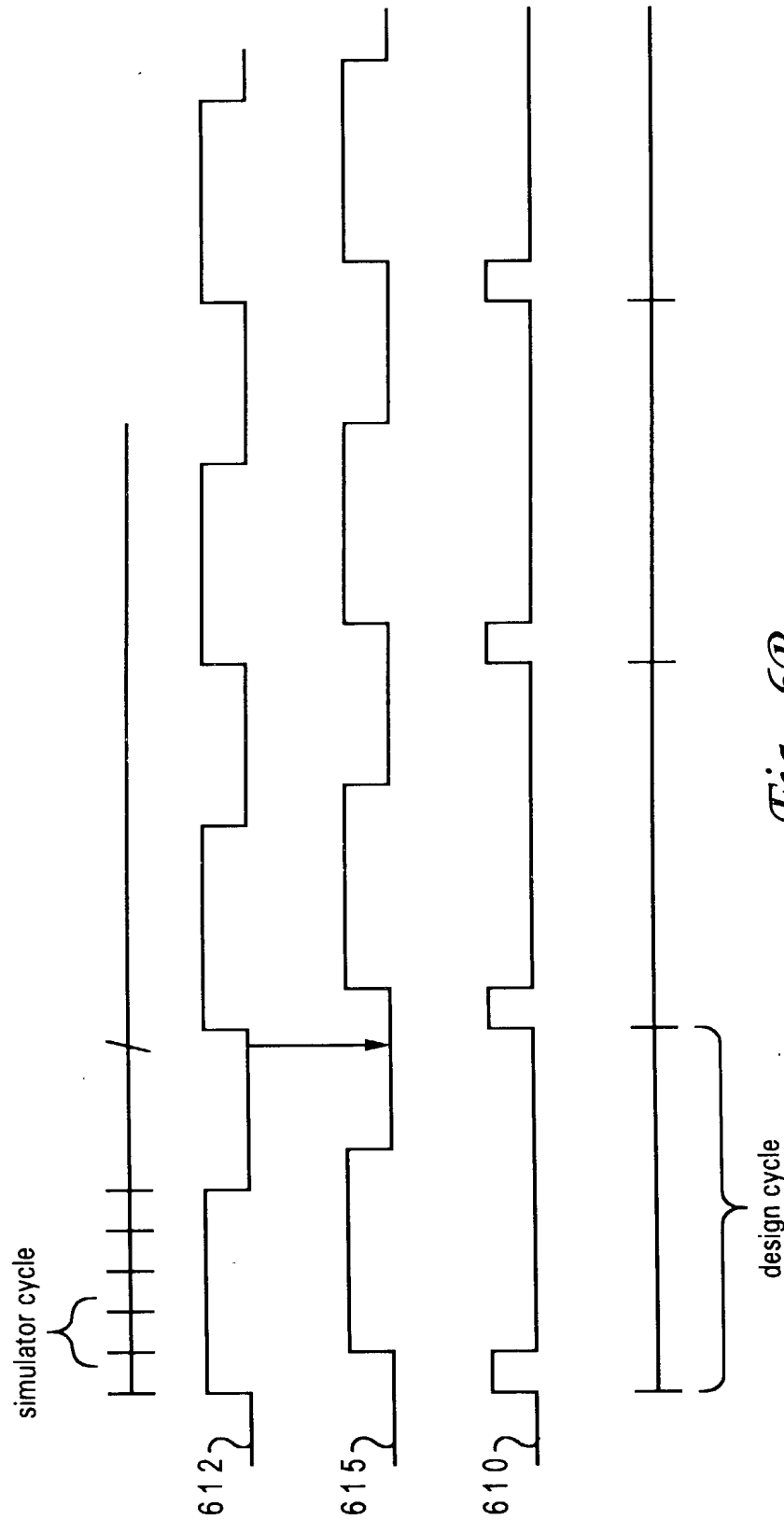


Fig. 6B

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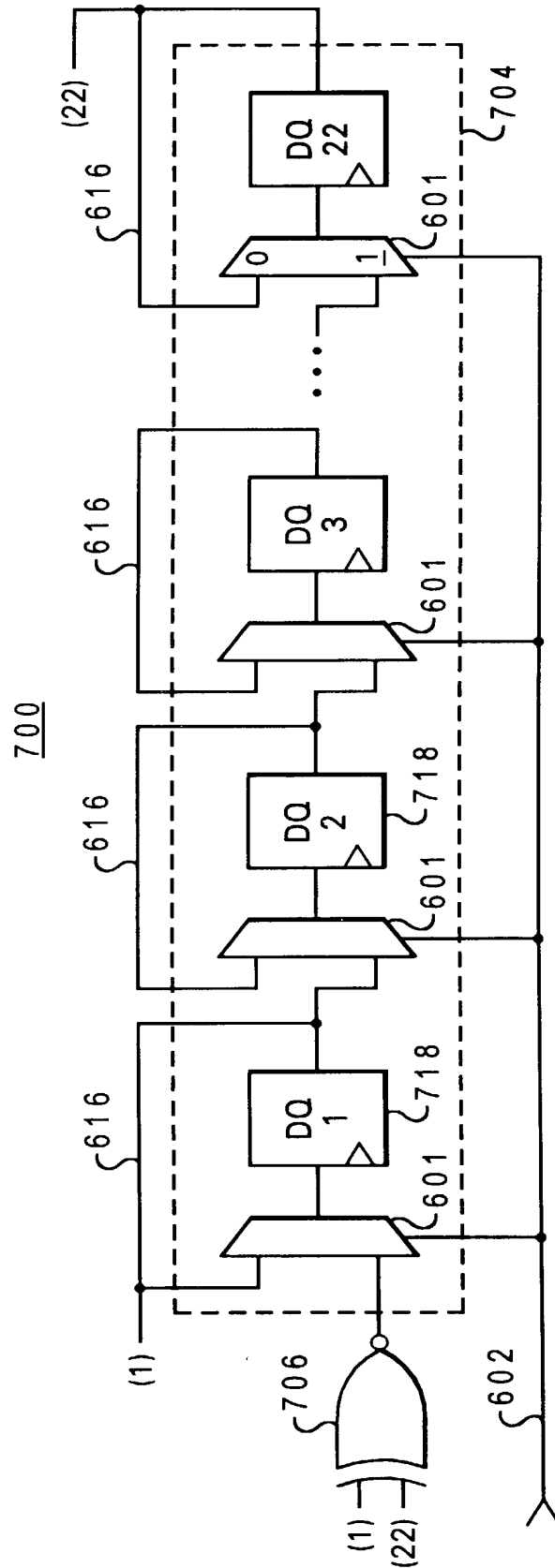


Fig. 7

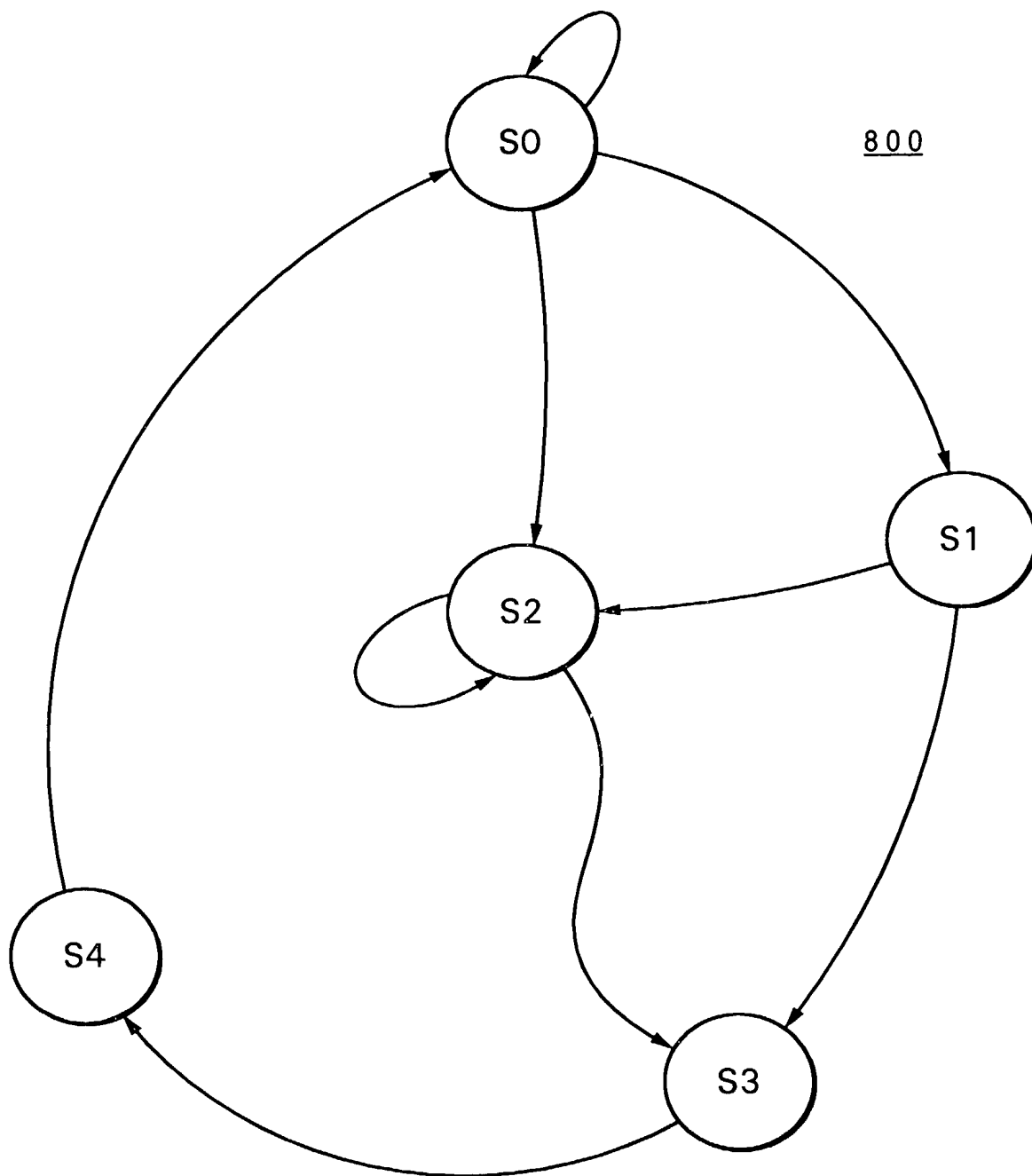


Fig. 8A
Prior Art

entity FSM : FSM

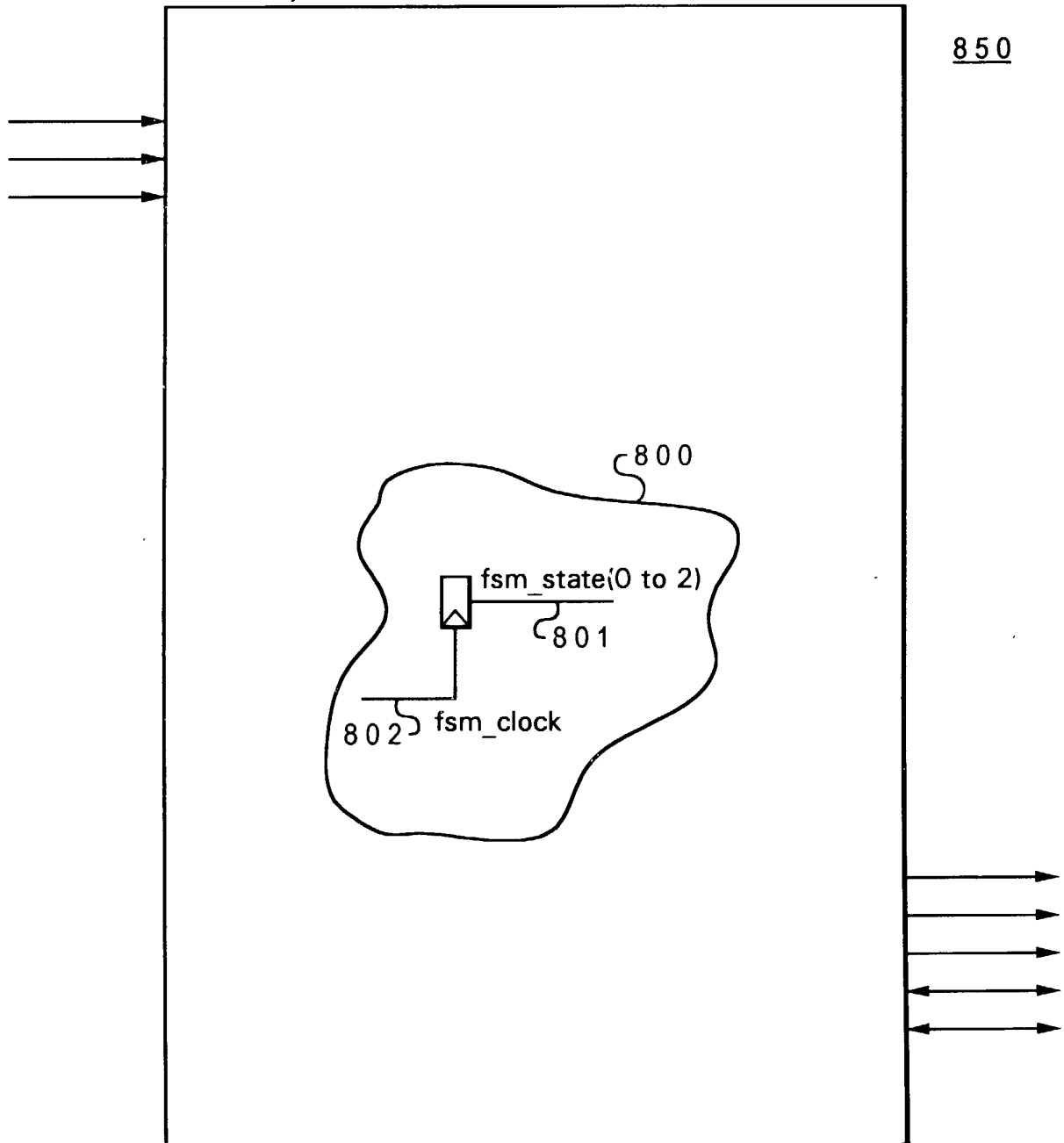


Fig. 8B

Prior Art

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ENTITY FSM IS

PORT(
 ports for entity fsm....
);

ARCHITECTURE FSM OF FSM IS

BEGIN

 ... HDL code for FSM and rest of the entity ...

 fsm_state(0 to 2) <= ... Signal 801 ...

8 5 3 { 8 5 9 { 8 5 4 { 8 5 5 { 8 5 6 { 8 5 7 { 8 5 8 {	--!! Embedded FSM : examplefsm; --!! clock : (fsm_clock); --!! state_vector : (fsm_state(0 to 2)); --!! states : (S0, S1, S2, S3, S4); --!! state_encoding : ('000', '001', '010', '011', '100'); --!! arcs : (S0 => S0, S0 => S1, S0 => S2, --!! (S1 => S2, S1 => S3, S2 => S2, --!! (S2 => S3, S3 => S4, S4 => S0); --!! End FSM;	} } } } } } }	8 5 2 } 8 6 0
---	---	---------------------------------	---------------

END;

Fig. 8C

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entity FSM : FSM

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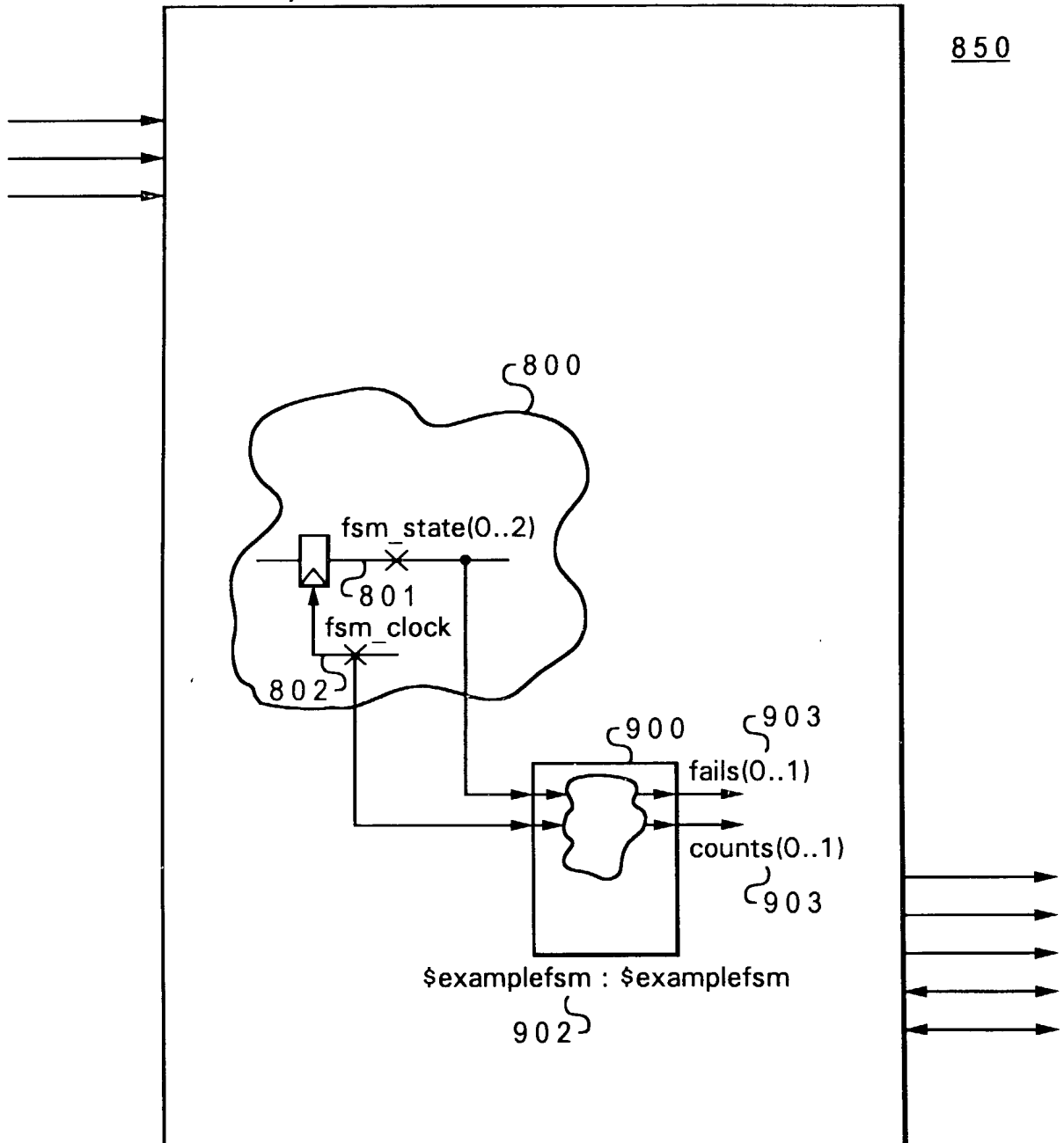
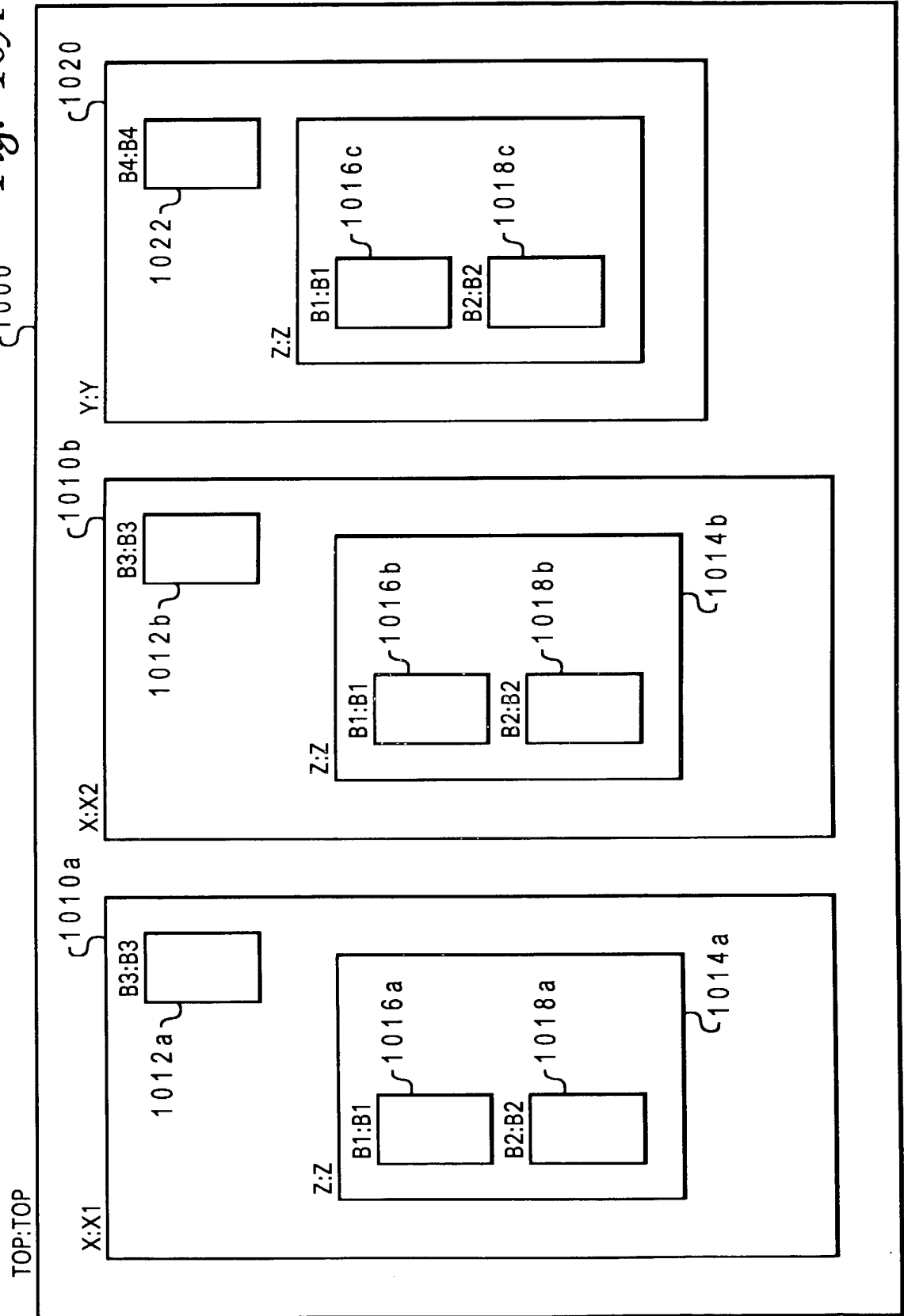


Fig. 9

Fig. 10A



1030 1032 1034 1036
<instantiation identifier> . <instrumentation entity name> . <design entity name> . <eventname>

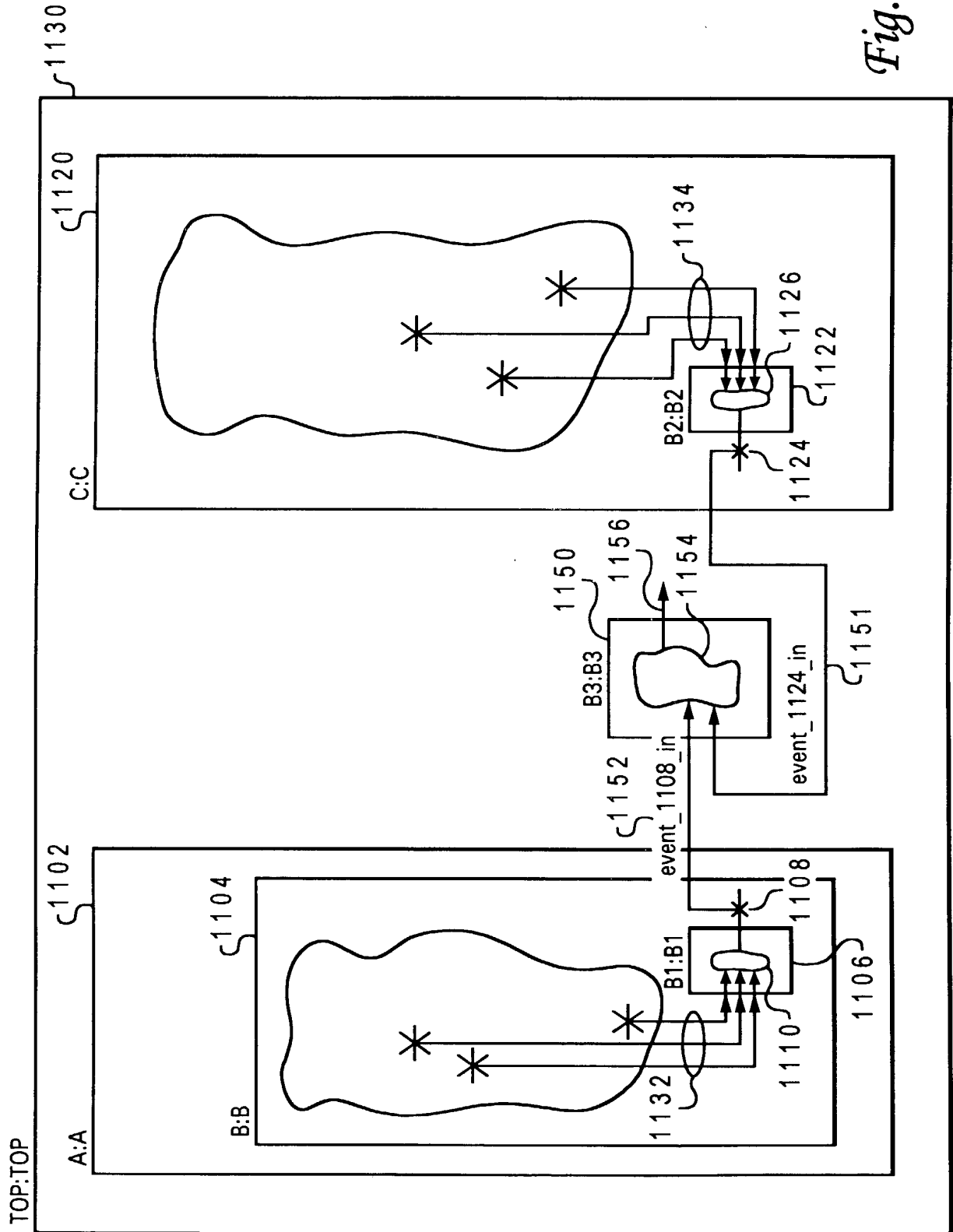
Fig. 10B

X1	B3	X	COUNT1
X1.Z	B1	Z	COUNT1
X1.Z	B2	Z	COUNT1
X2	B3	X	COUNT1
X2.Z	B1	Z	COUNT1
X2.Z	B2	Z	COUNT1
Y	B4	Y	COUNT1
Y.Z	B1	Z	COUNT1
Y.Z	B2	Z	COUNT1

Fig. 10C

1030 1034 1036
<instantiation identifier> . <design entity name> . <eventname>

Fig. 10D



--!! Inputs
 --!! event_1108_in <= C.[B2.count.event_1108];
 --!! event_1124_in <= A.B.[B1.count.event_1124];
 --!! End Inputs

1163 1165 1161 1162 1164 1166

Fig. 11B

--!! Inputs
 --!! event_1108_in <= C.[count.event_1108];
 --!! event_1124_in <= B.[count.event_1124];
 --!! End Inputs

1171 1172

Fig. 11C

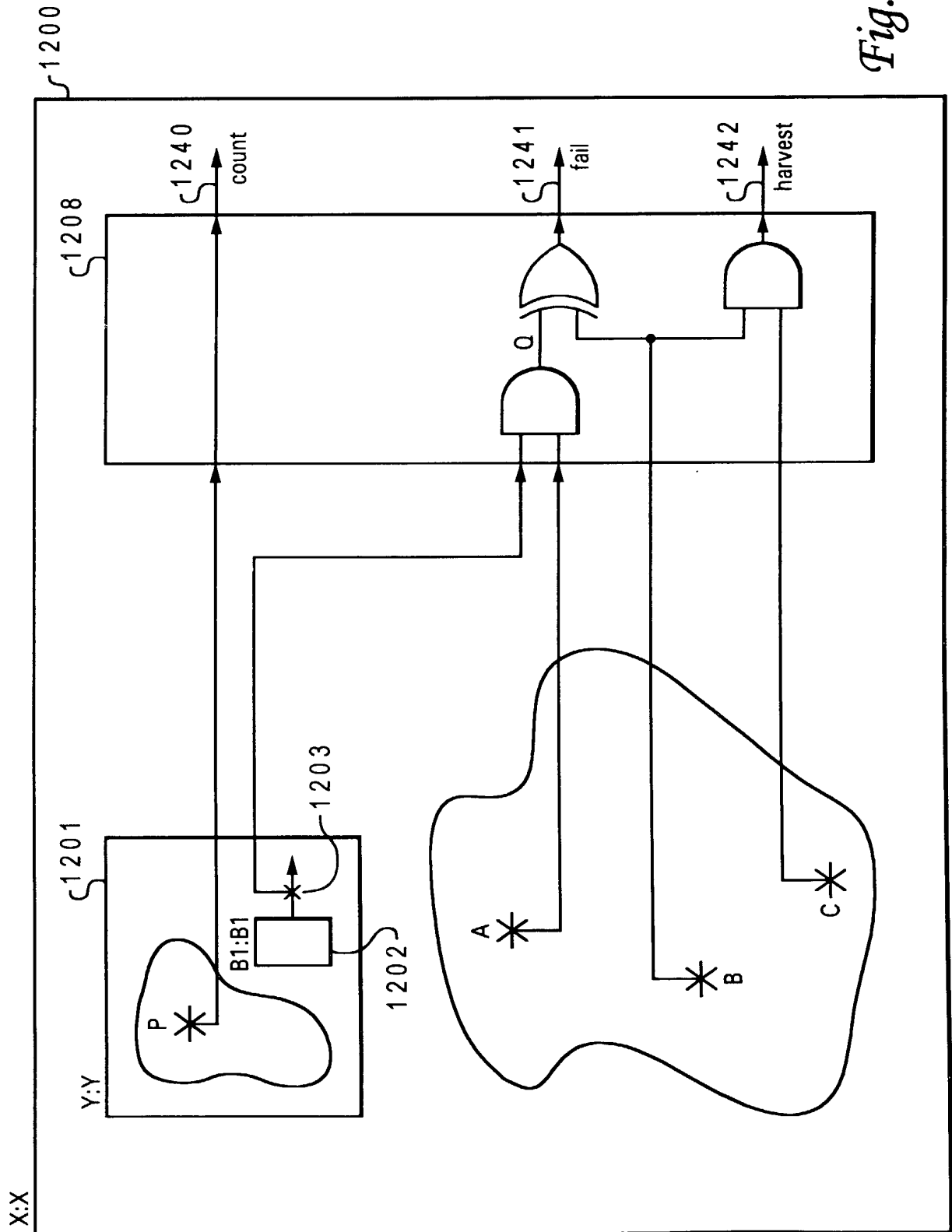


Fig. 12B

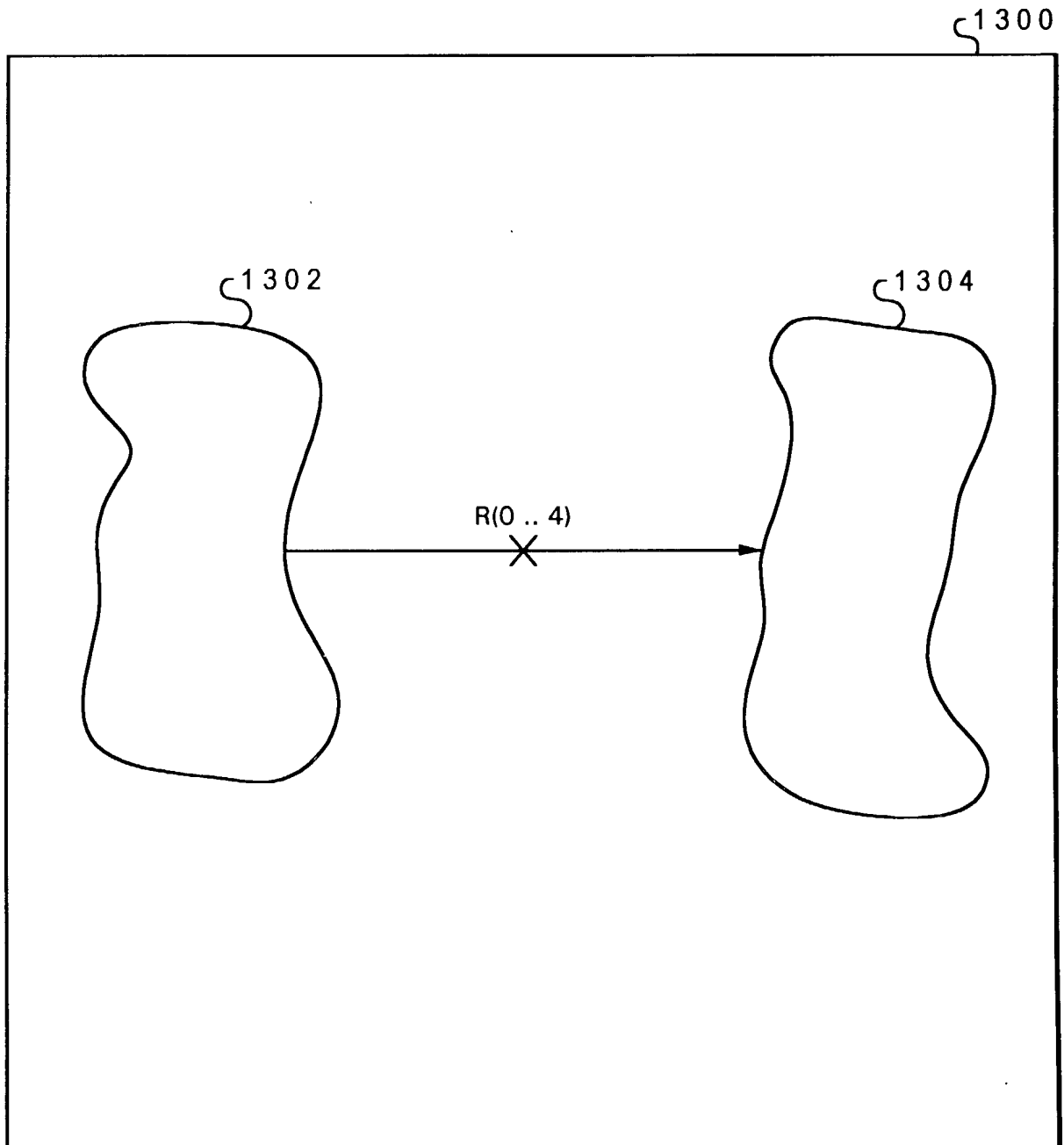


Fig. 13A

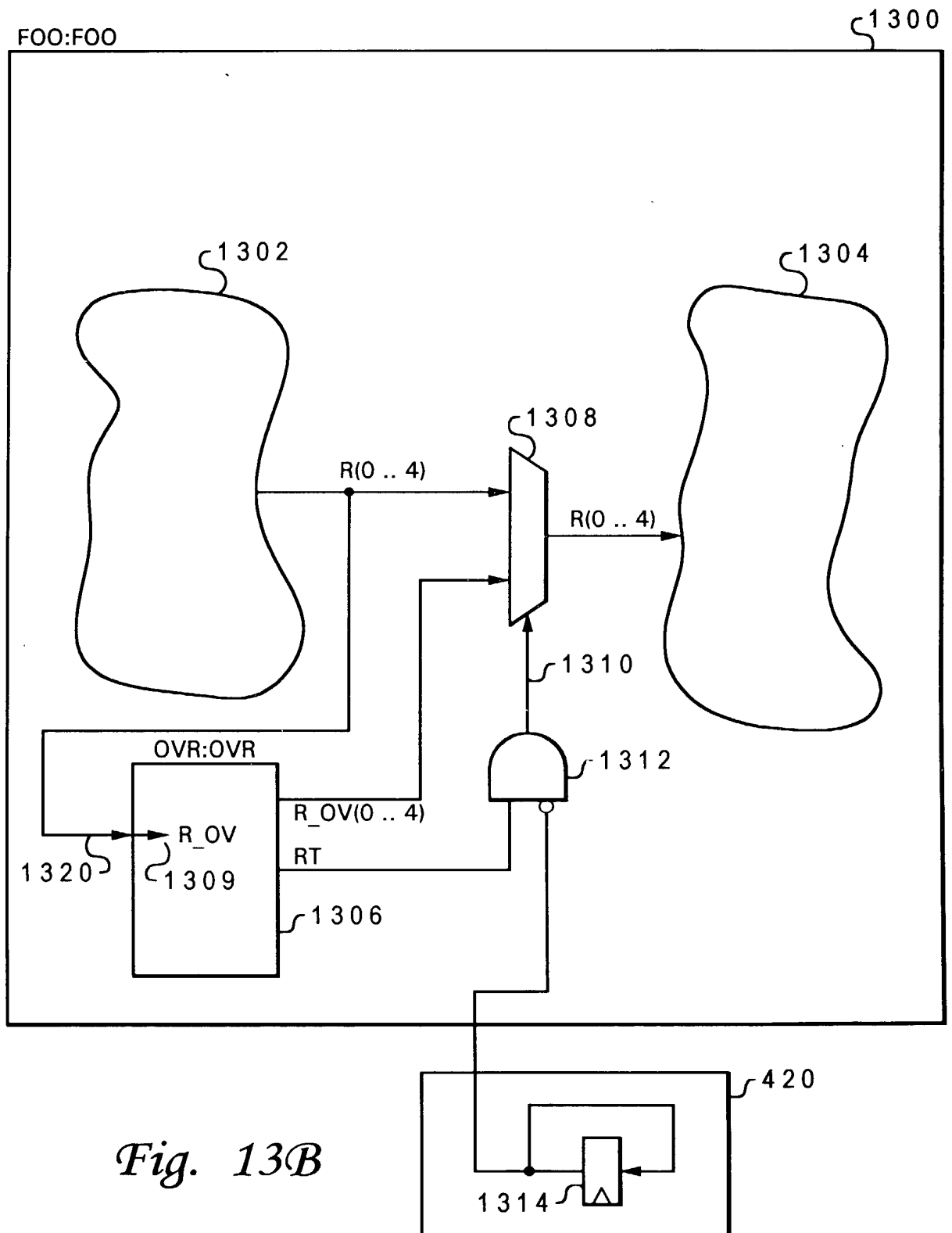


Fig. 13B

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```

ENTITY OVR IS
    PORT(  R_IN      :  IN std_ulogic_vector(0 .. 4);
           .
           .
           ... other ports as required ...
           .
           .
           R_OV      :  OUT std_ulogic_vector(0 .. 4);
           RT         :  OUT std_ulogic
    );

--!! BEGIN
--!! Design Entity: FOO;

--!! Inputs (0 to 4)
--!! R_IN => {R(0 .. 4)};
--!! :
--!! ... other ports as needed ...
--!! :
--!! End Inputs

--!! Outputs
--!! <R_OVRRIDE> : R_OV(0 .. 4) => R(0 .. 4) [RT];
--!! End Outputs

--!! End

ARCHITECTURE example of OVR IS
    BEGIN
        ... HDL code for entity body section ...
    END;
    
```

Handwritten annotations and brackets:

- 1364: A bracket grouping the `R_IN` input port.
- 1362: A bracket grouping the `R_OV` and `RT` output ports.
- 1363: A bracket grouping the `RT` output port.
- 1360: A bracket grouping the `R_IN` input port.
- 1361: A bracket grouping the `R_OV` output port.
- 1351: A bracket grouping the `RT` output port.
- 1356: A bracket grouping the `RT` output port.
- 1340: A bracket grouping the `RT` output port.
- 1358: A bracket grouping the `RT` output port.

Fig. 13C

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ENTITY FOO IS

PORT(:
:
:
);

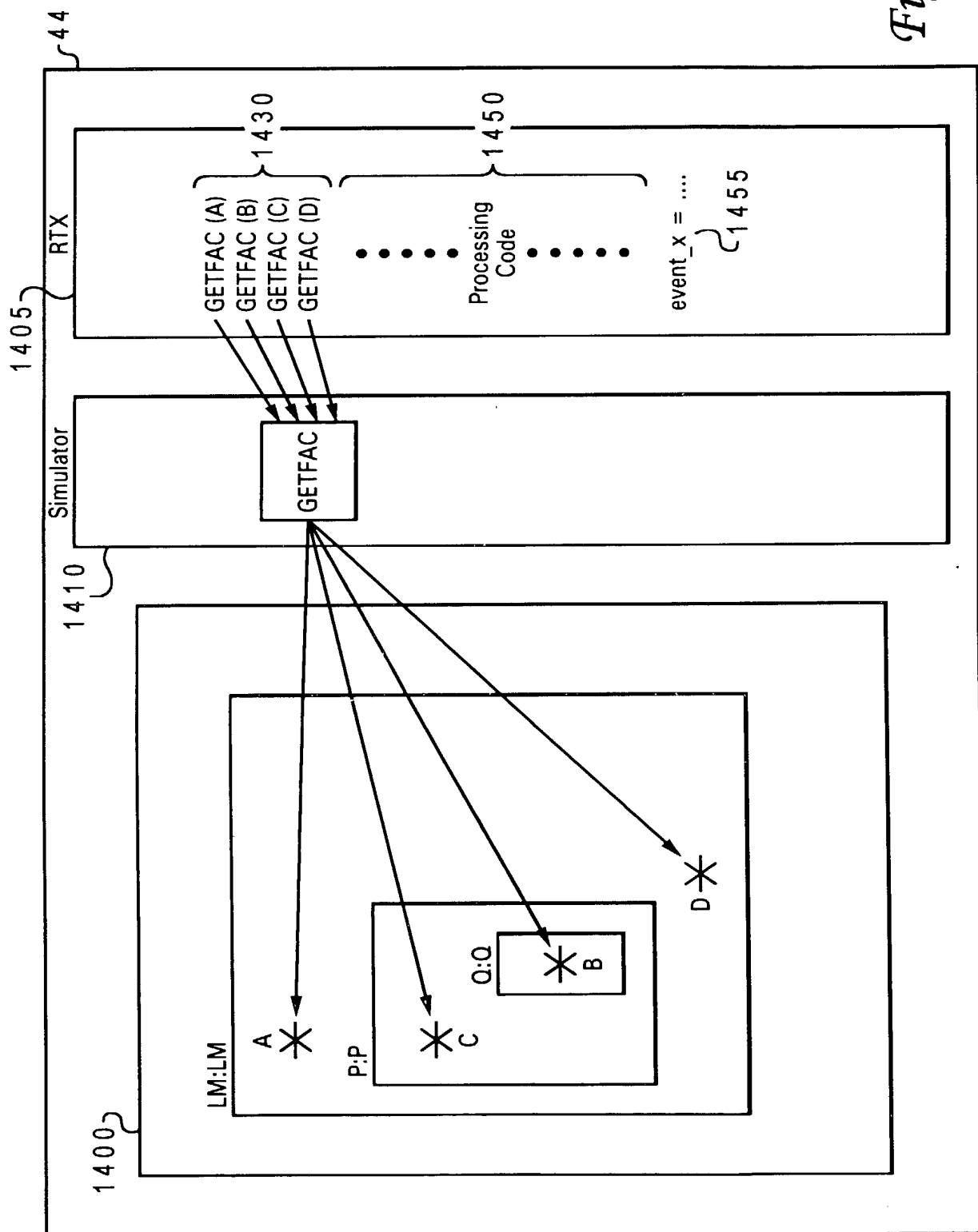
ARCHITECTURE example of FOO IS

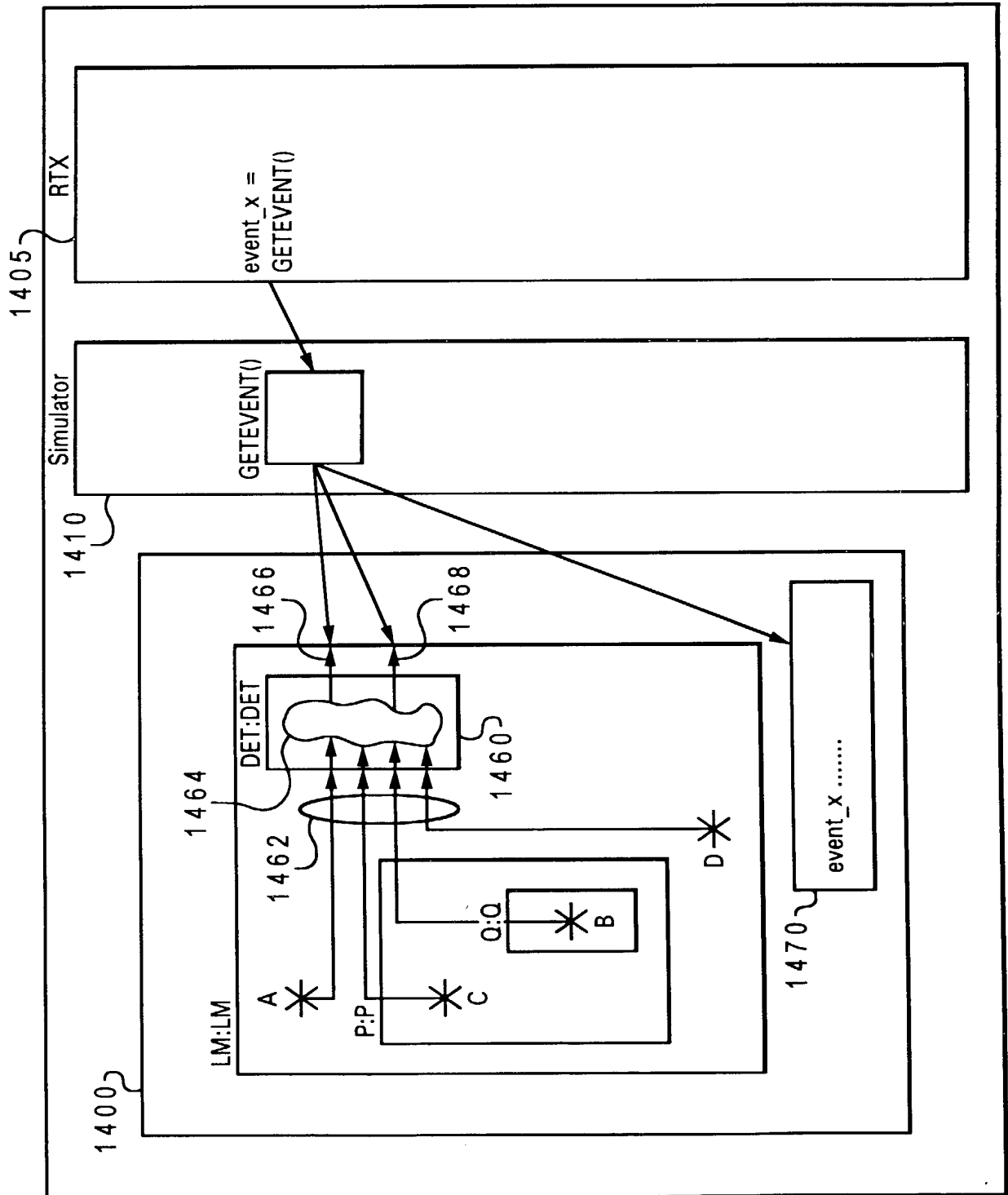
BEGIN

.
.
.
.
.
R <=
.
.
.
.

1380 { --!! R_IN <= {R}; 1381
--!! 1382
--!!
--!! R_OV(0 to 4) <=; 1383
--!! RT <=;
--!! [override, R_OVRRIDE, R(0 .. 4), RT] <= R_OV(0 to 4);
1384

Fig. 13D






```

ENTITY DET IS
    PORT(
        A      : IN std_ulogic;
        B      : IN std_ulogic_vector(0 to 5);
        C      : IN std_ulogic;
        D      : IN std_ulogic;
        :
        :
        event_x : OUT std_ulogic_vector(0 to 2);
        x_here  : OUT std_ulogic;
    );

    --!! BEGIN
    --!! Design Entity: LM;

    --!! Inputs
    --!! A  => A;
    --!! B  => P.Q.B;
    --!! C  => P.C;
    --!! D  => D;
    --!! End Inputs

    --!! Detections
    --!! <event_x>:event_x(0 to 2) [x_here];
    --!! End Detections

    --!! End;

    ARCHITECTURE example of DET IS
    BEGIN
        ... HDL code ...

    END;

```

1491 {

1493 {

1495 {

1494 {

1480 {

1492 {

Fig. 14C

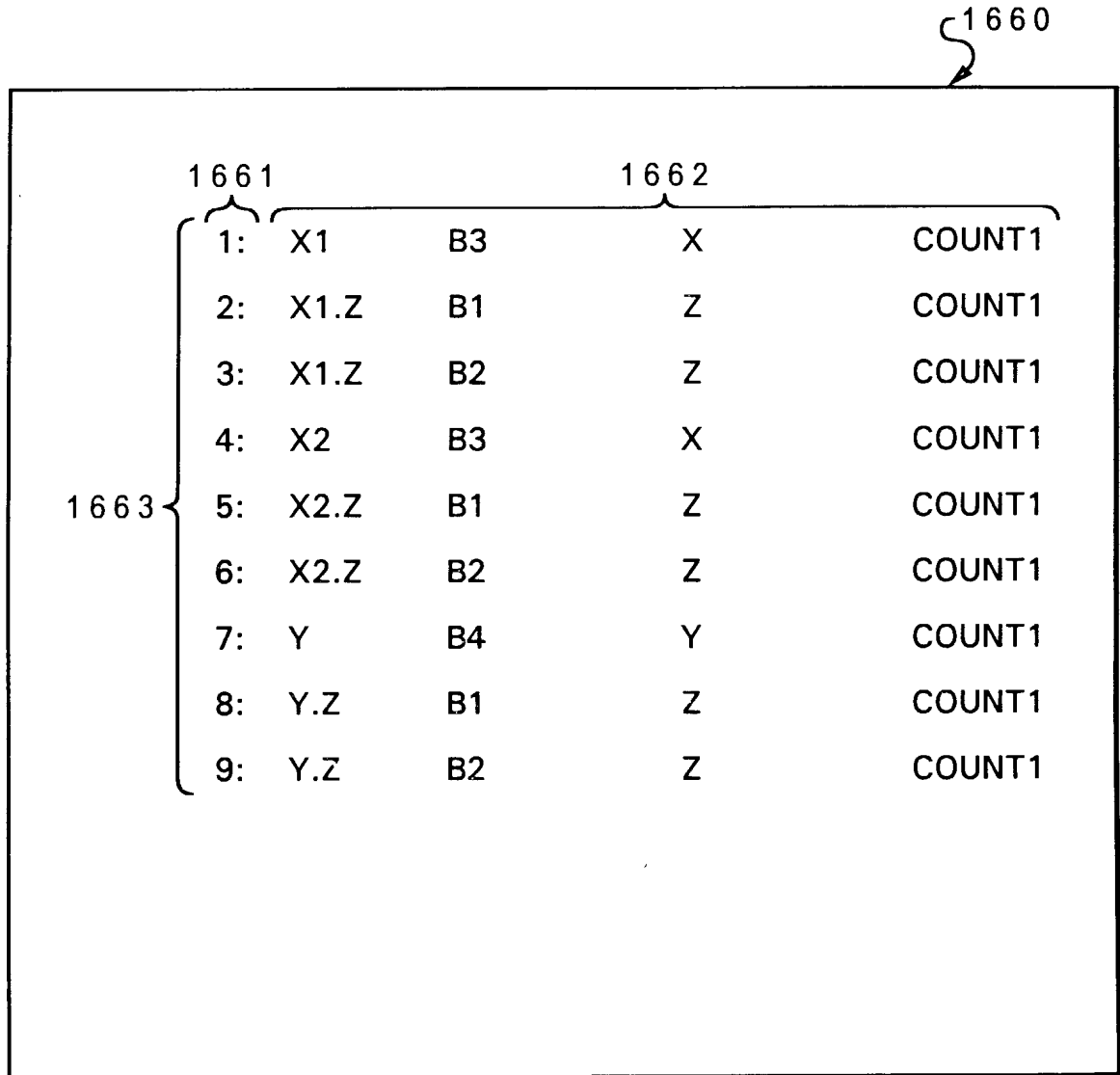
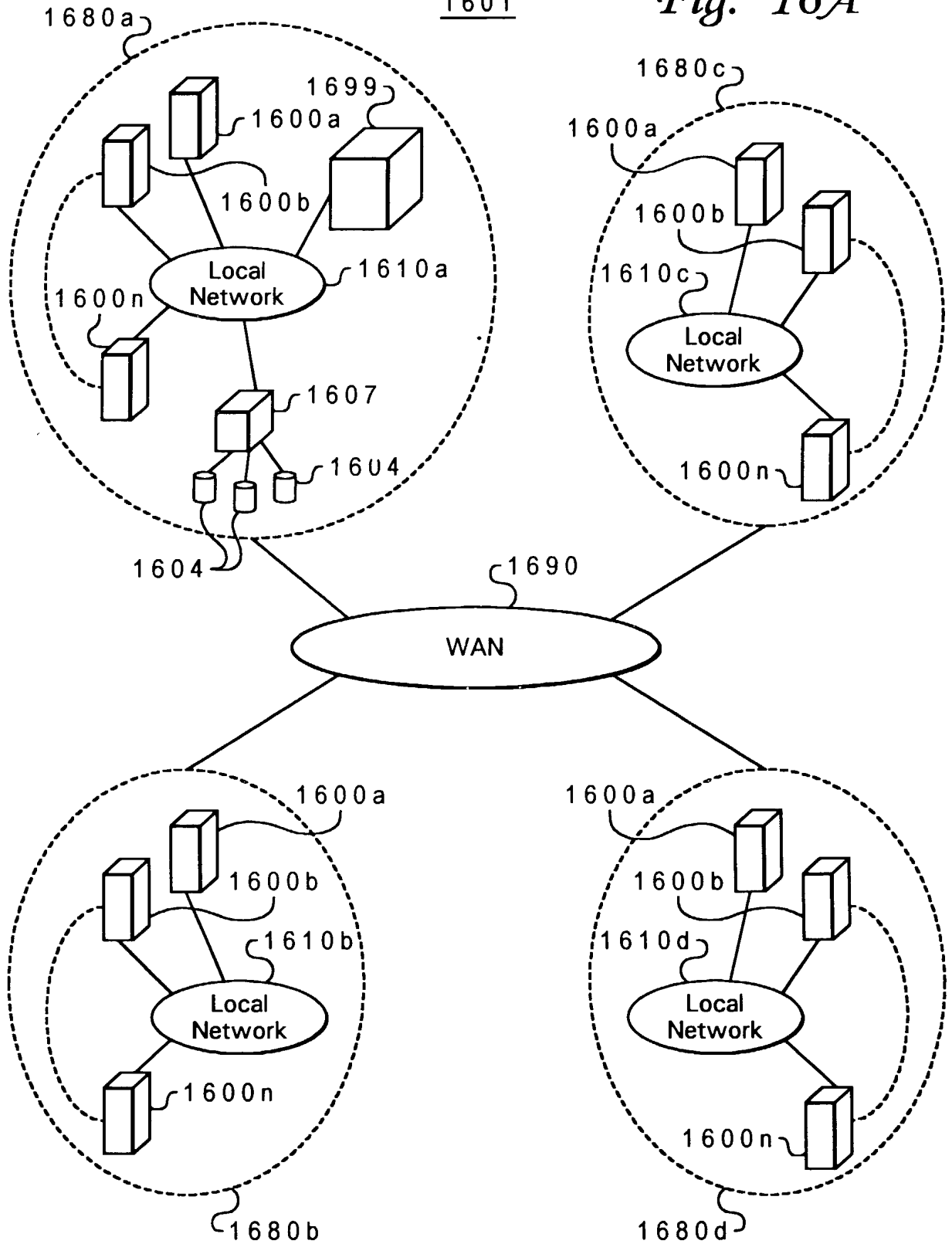


Fig. 15

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Fig. 16A



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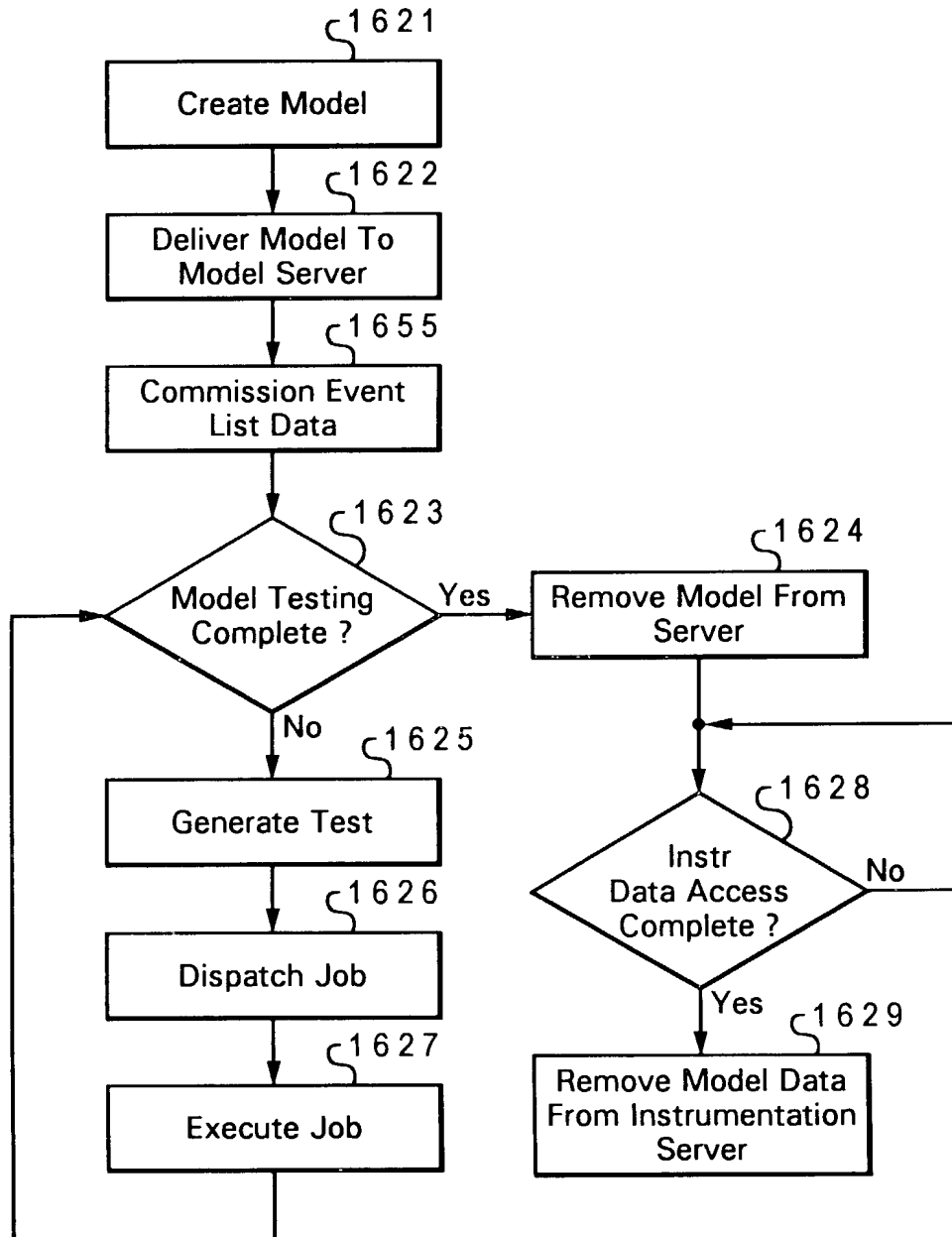


Fig. 16B

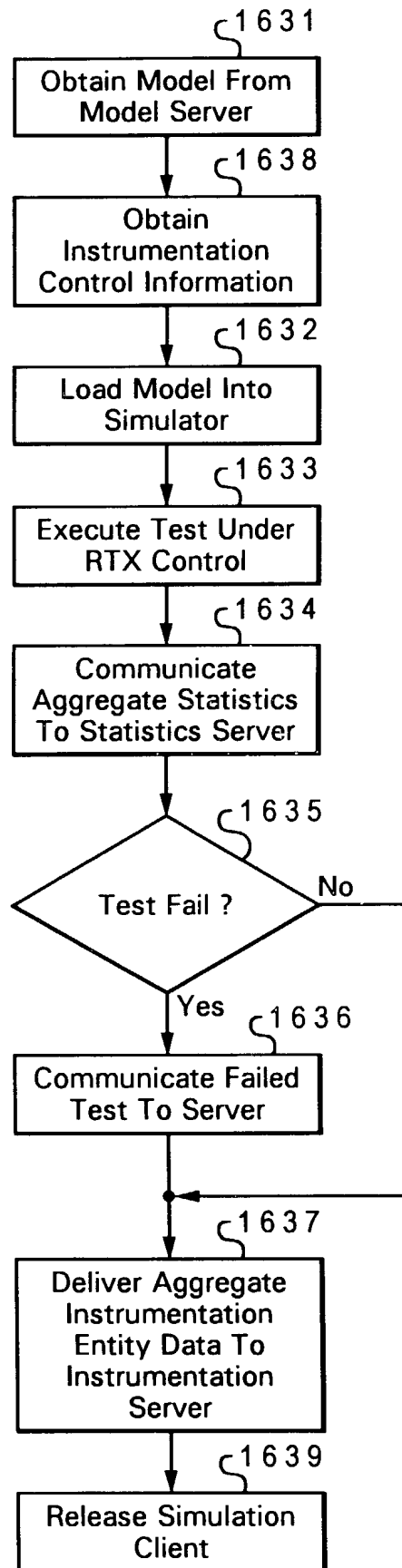


Fig. 16C

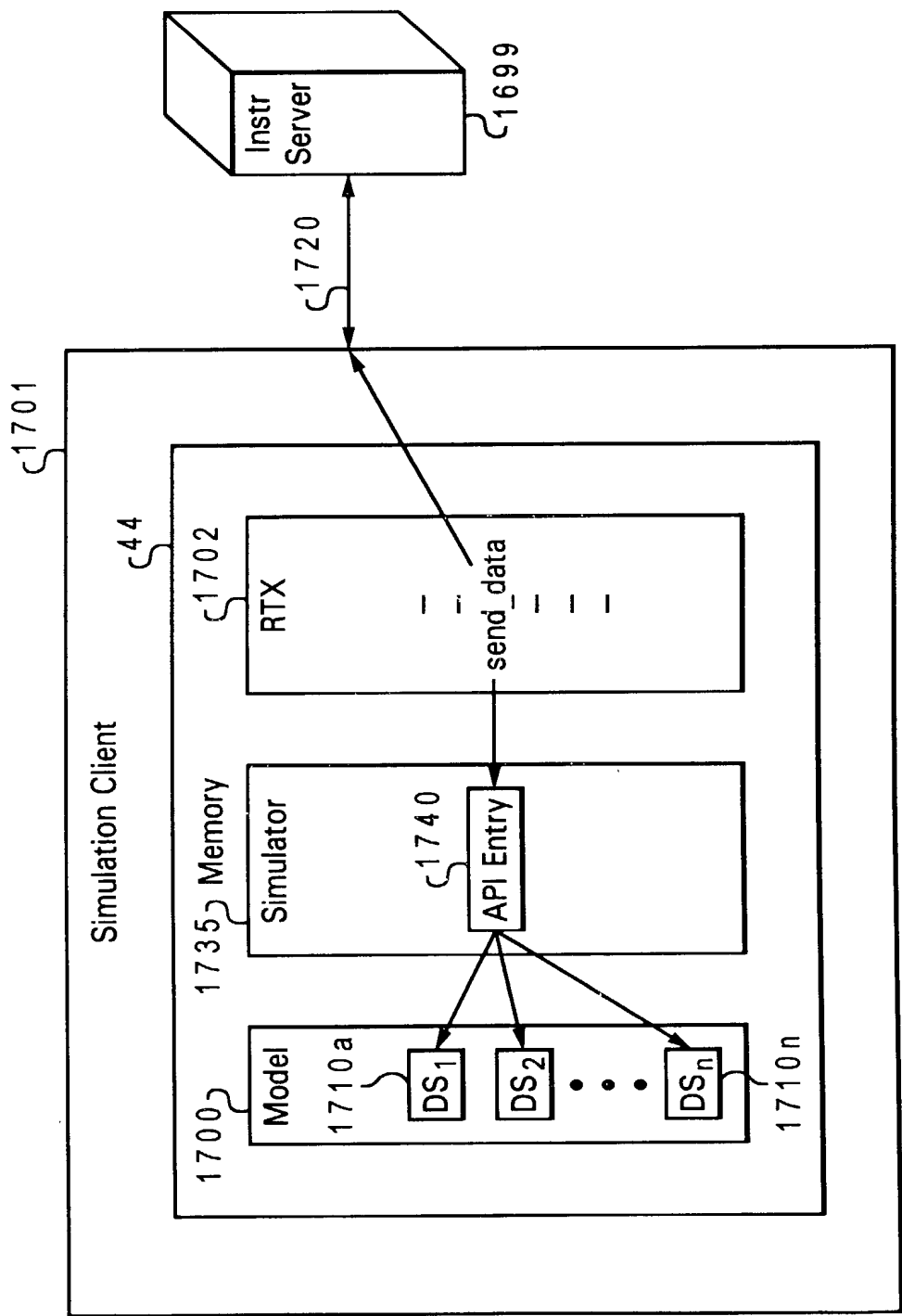


Fig. 17A

1750

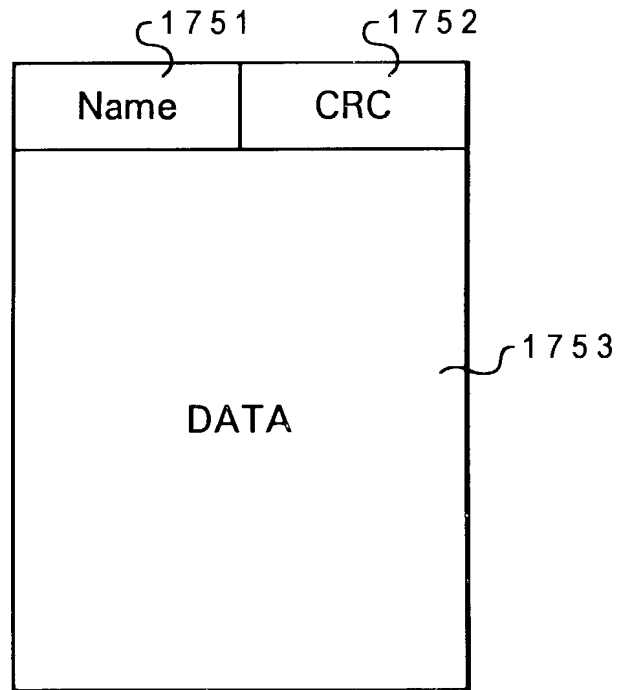


Fig. 17B

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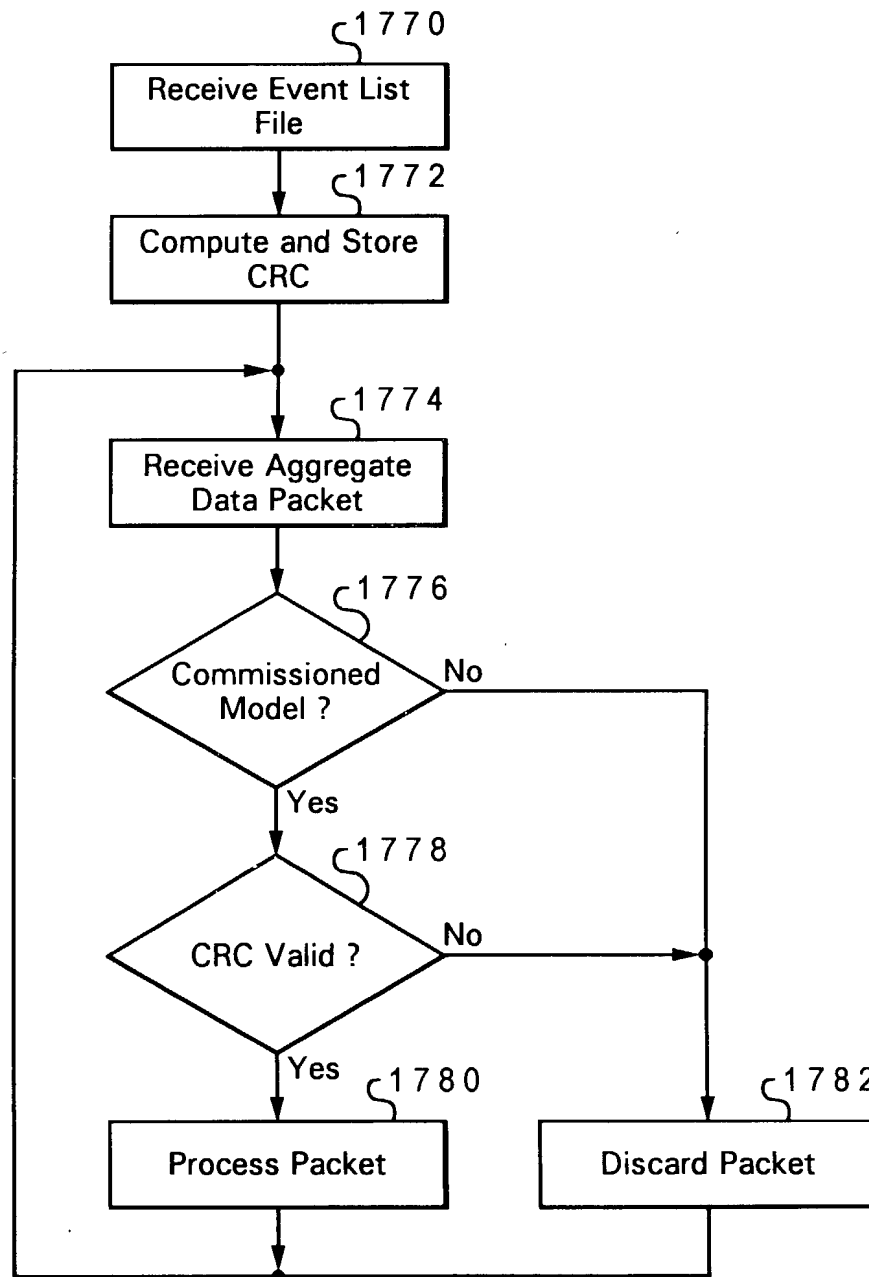


Fig. 17C

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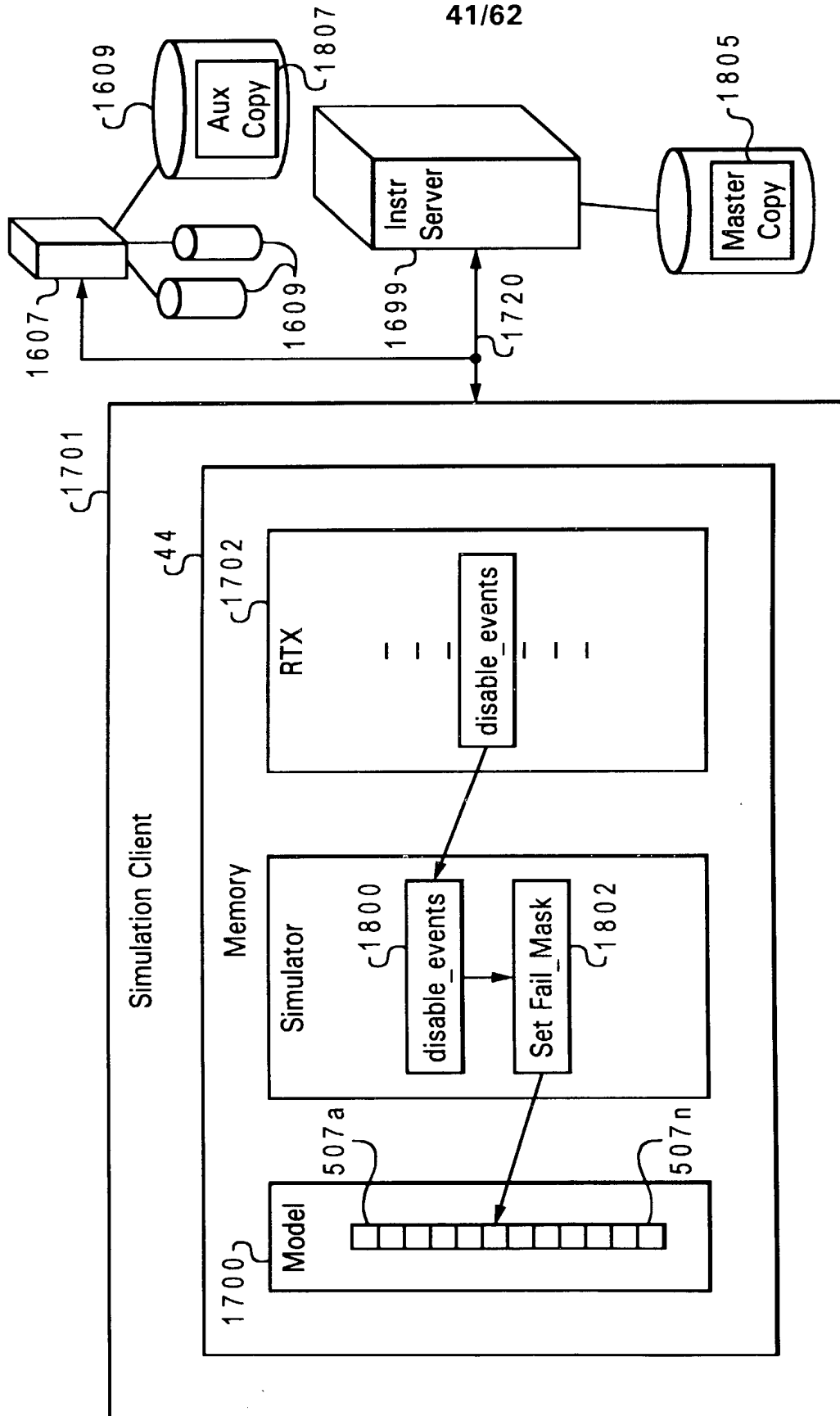
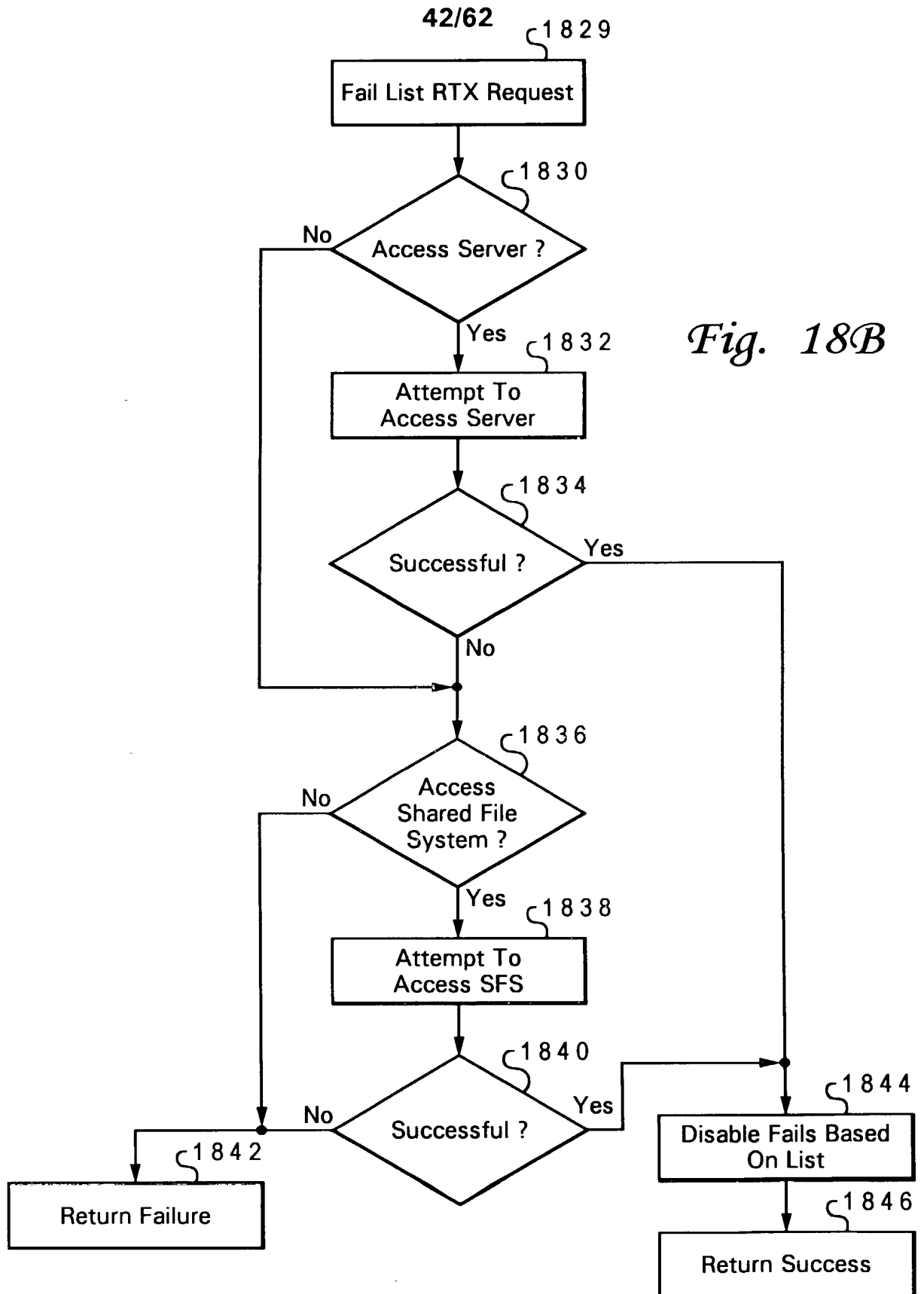


Fig. 18A



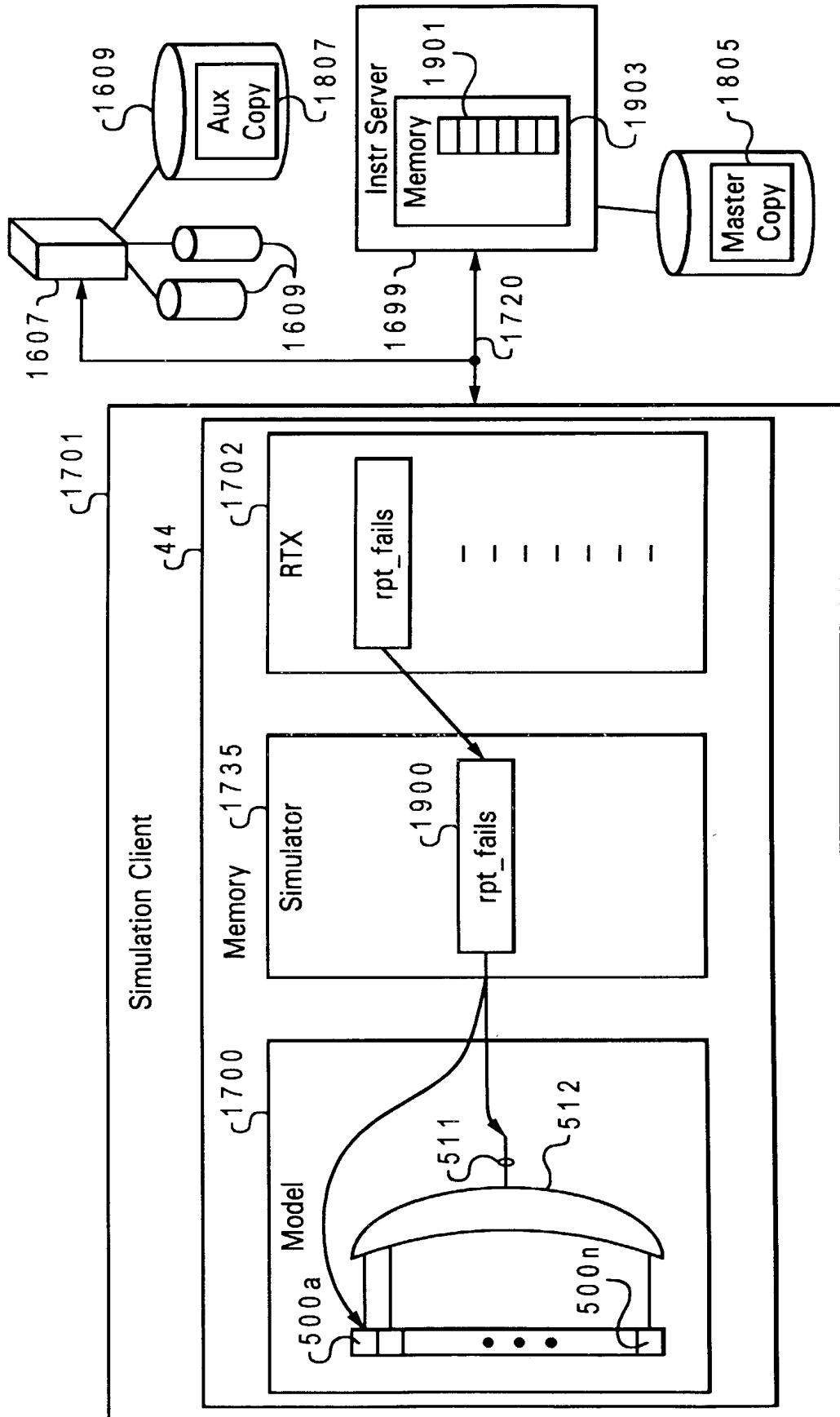
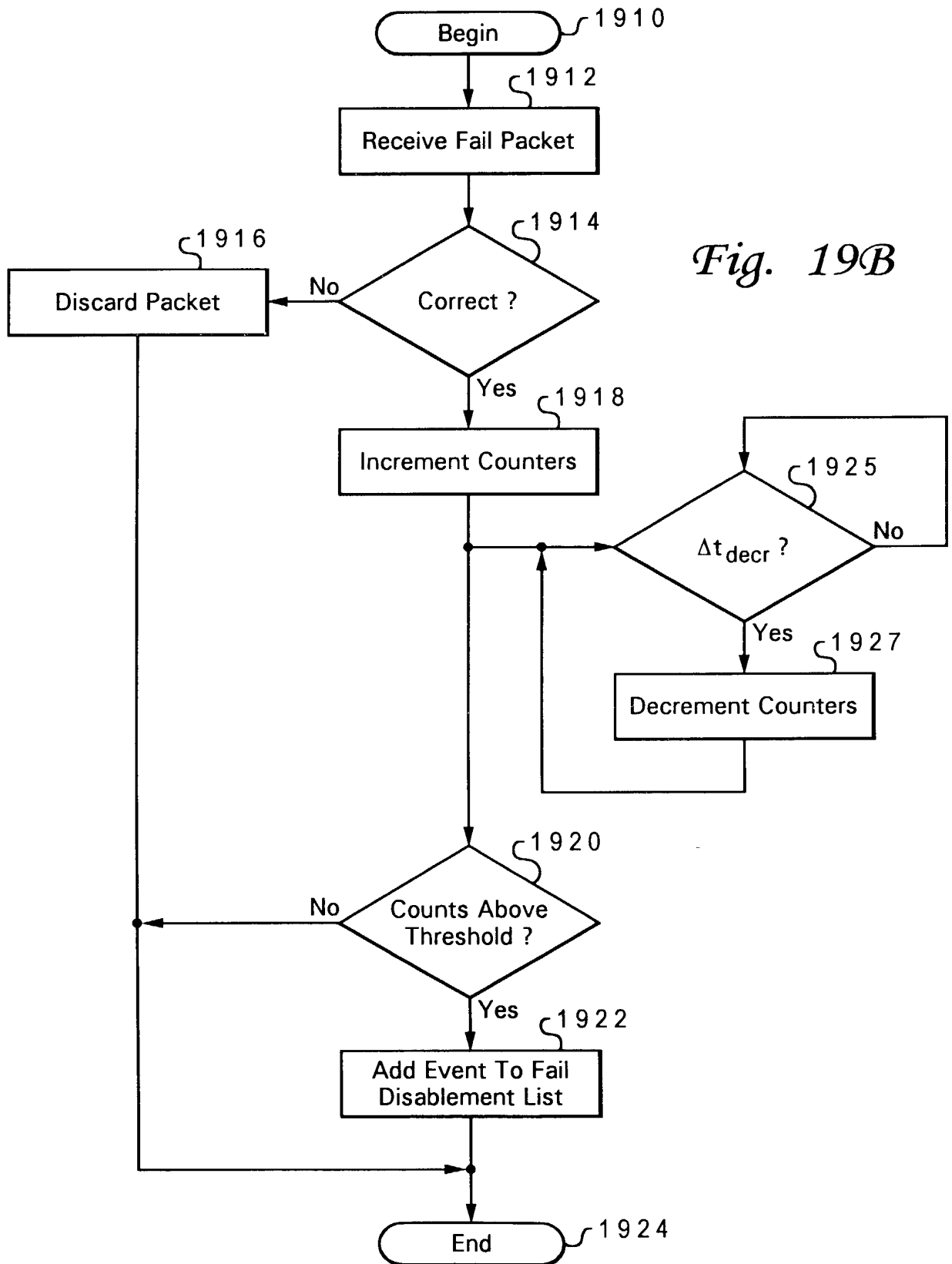


Fig. 19A

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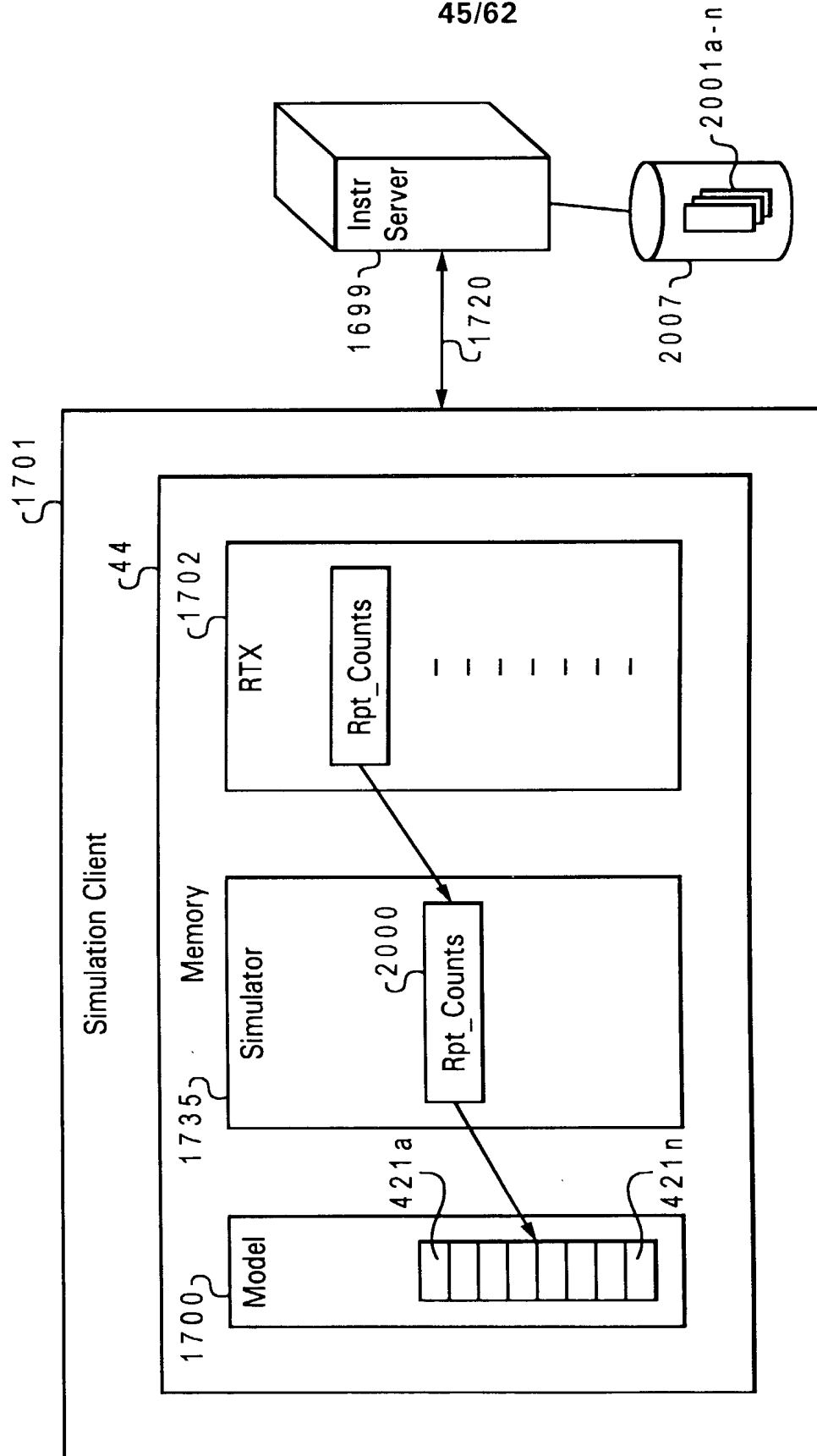


Fig. 20A

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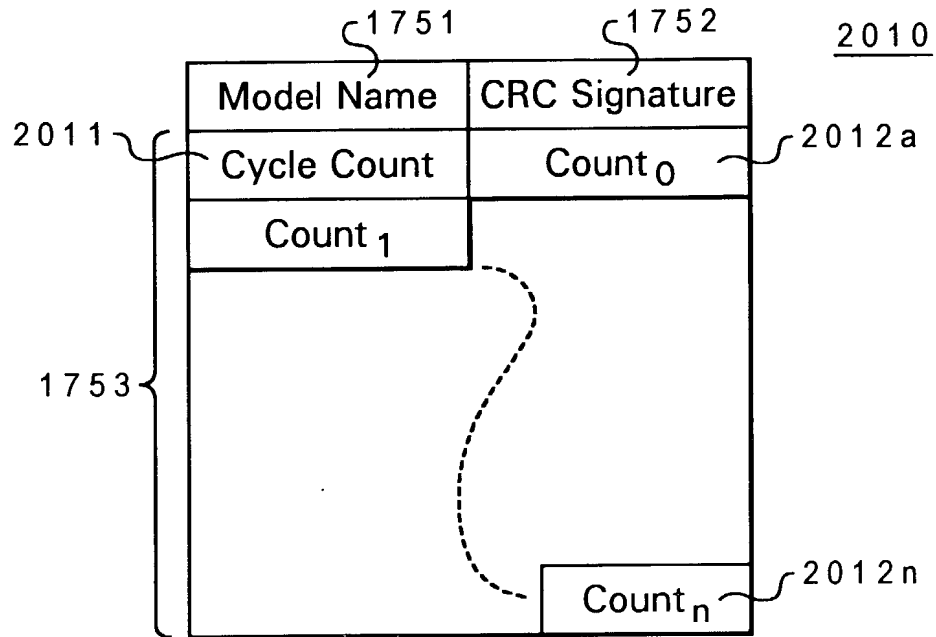


Fig. 20B

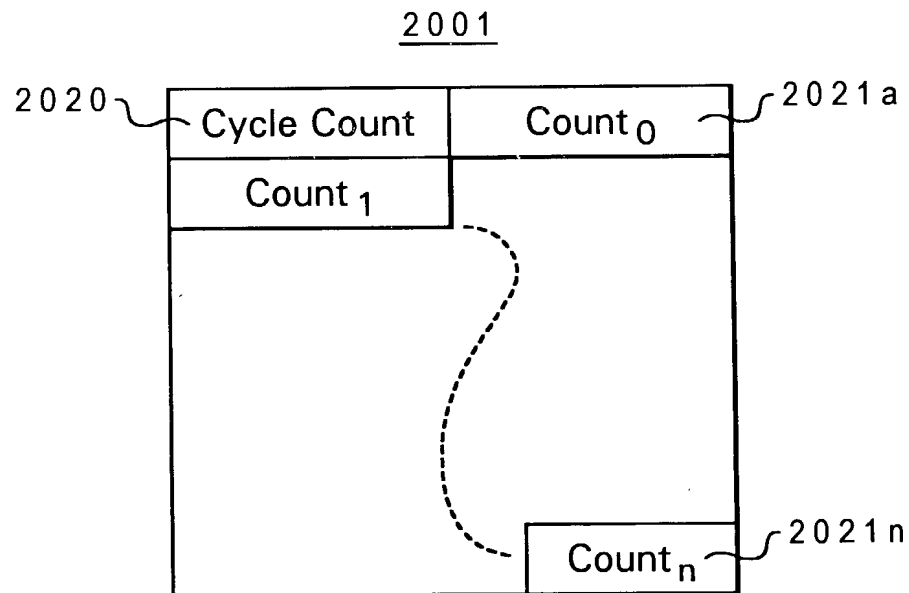


Fig. 20C

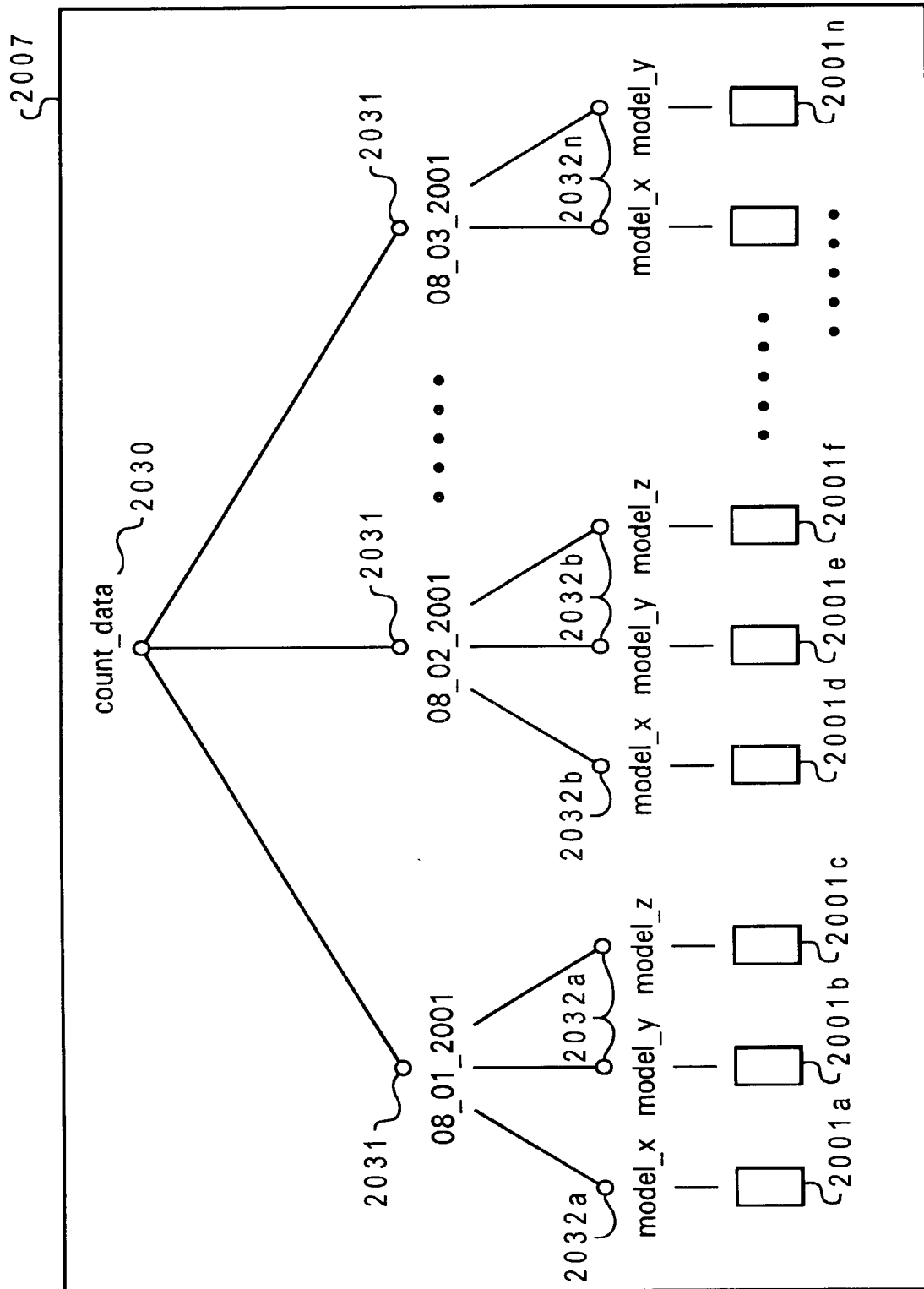


Fig. 20D

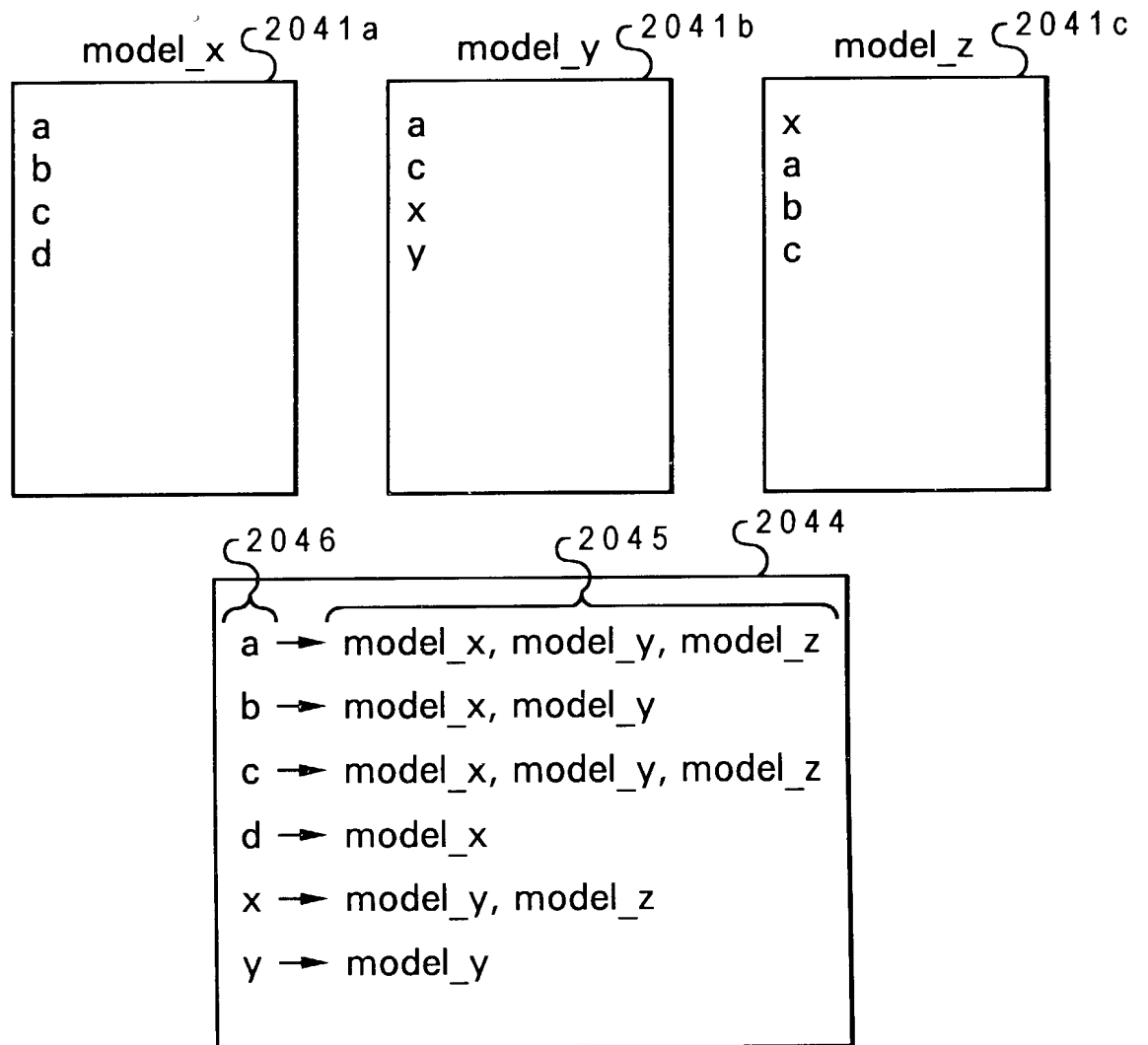


Fig. 20E

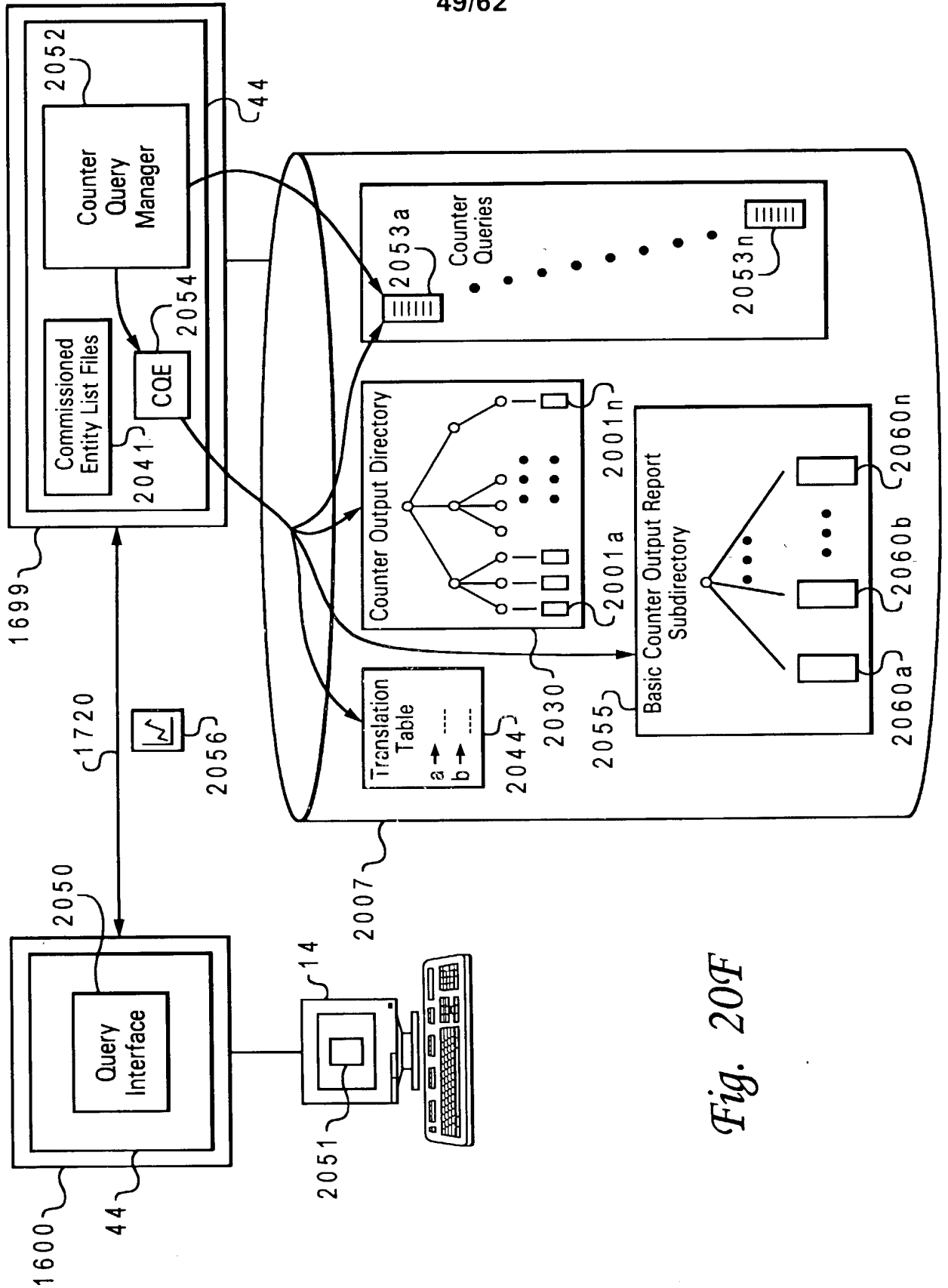
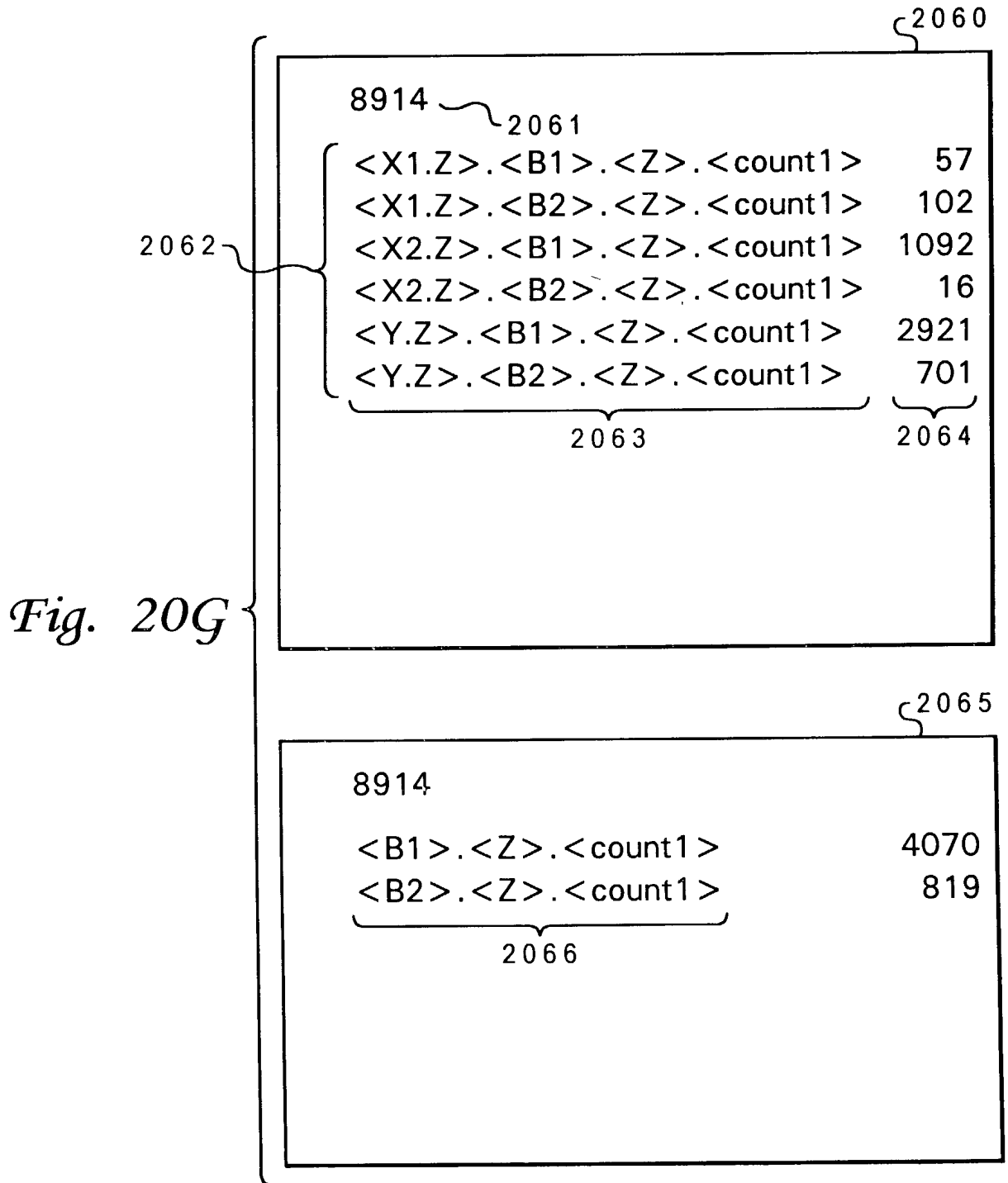


Fig. 20F



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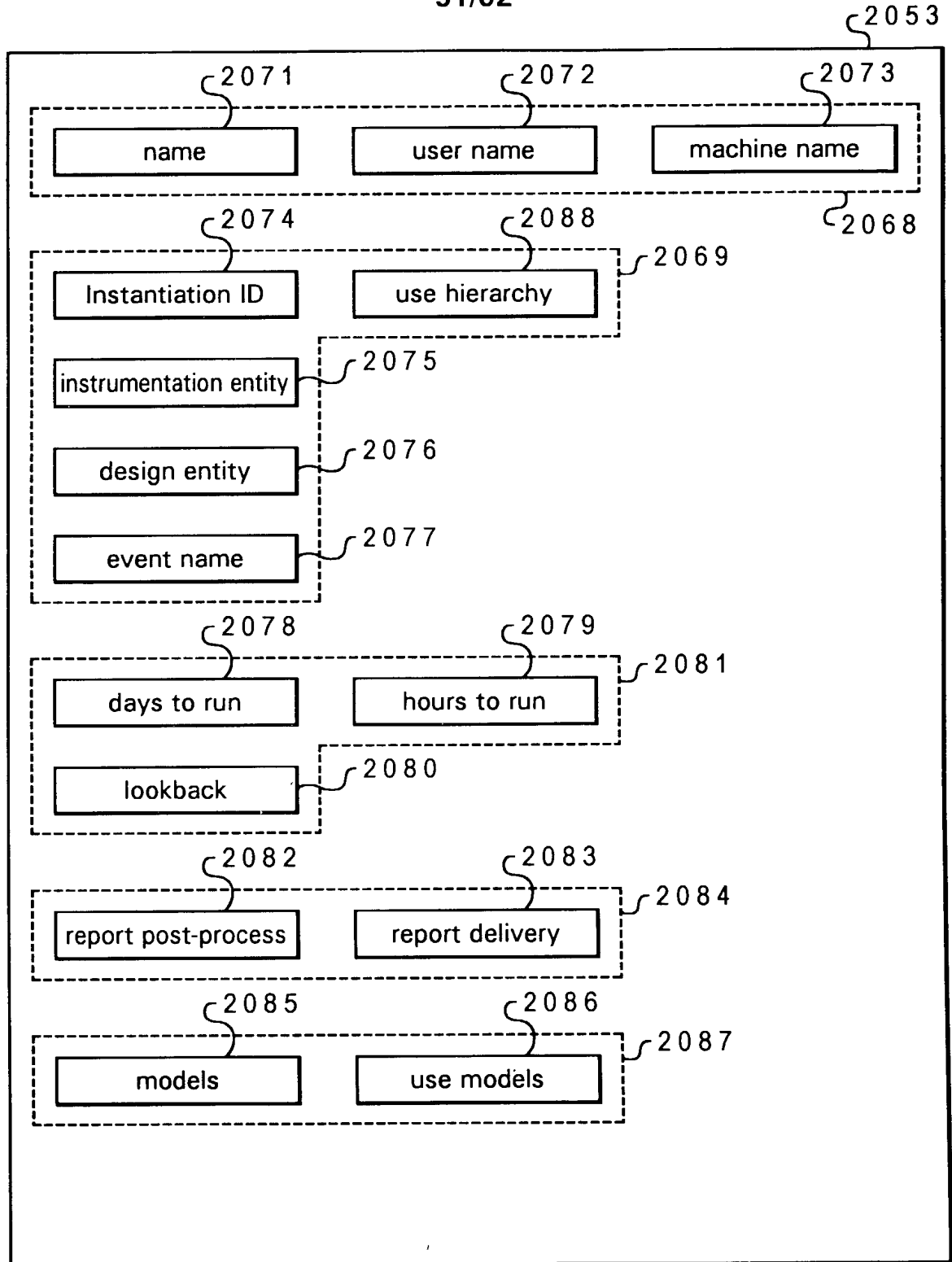


Fig. 20H

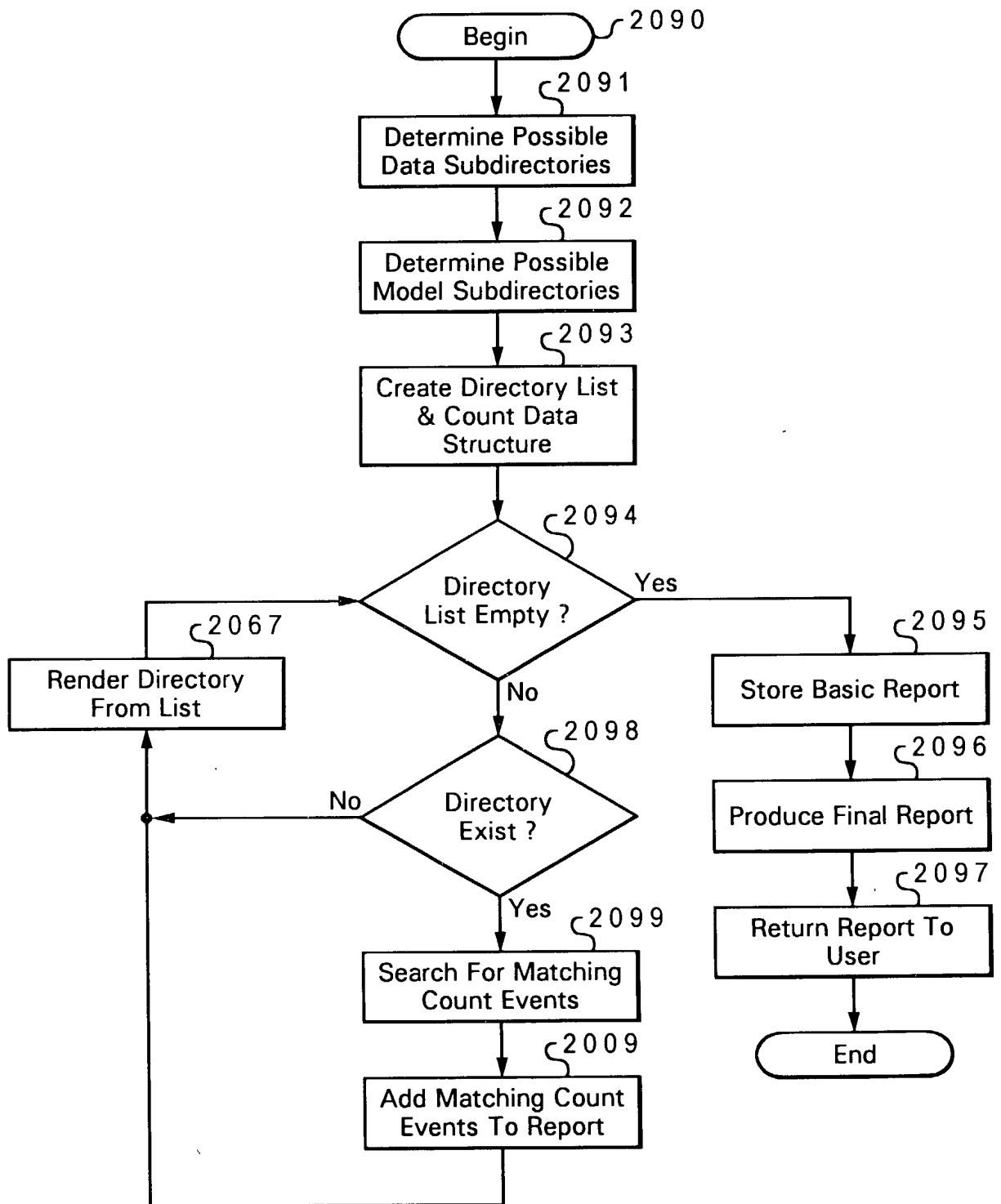


Fig. 20I

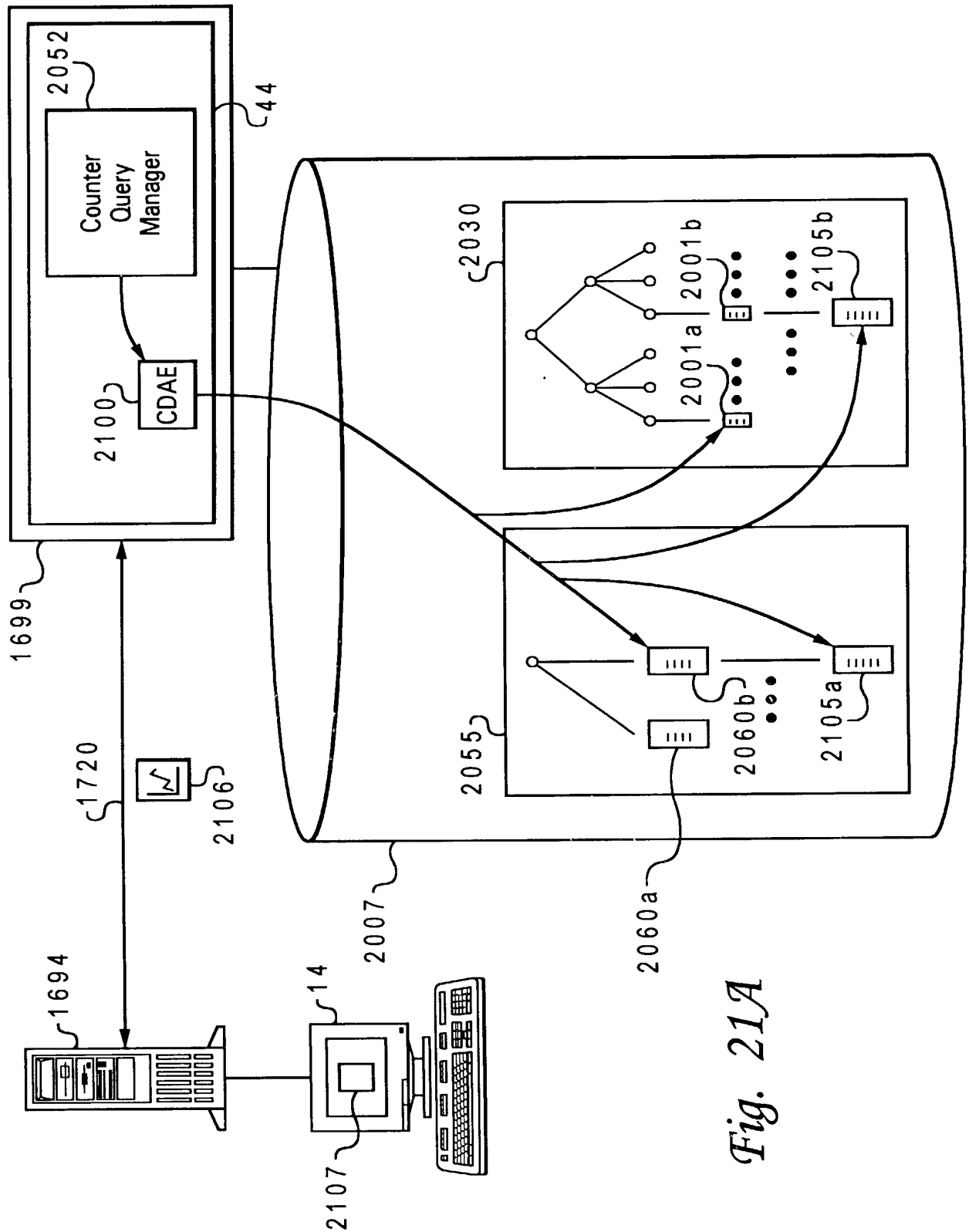


Fig. 21A

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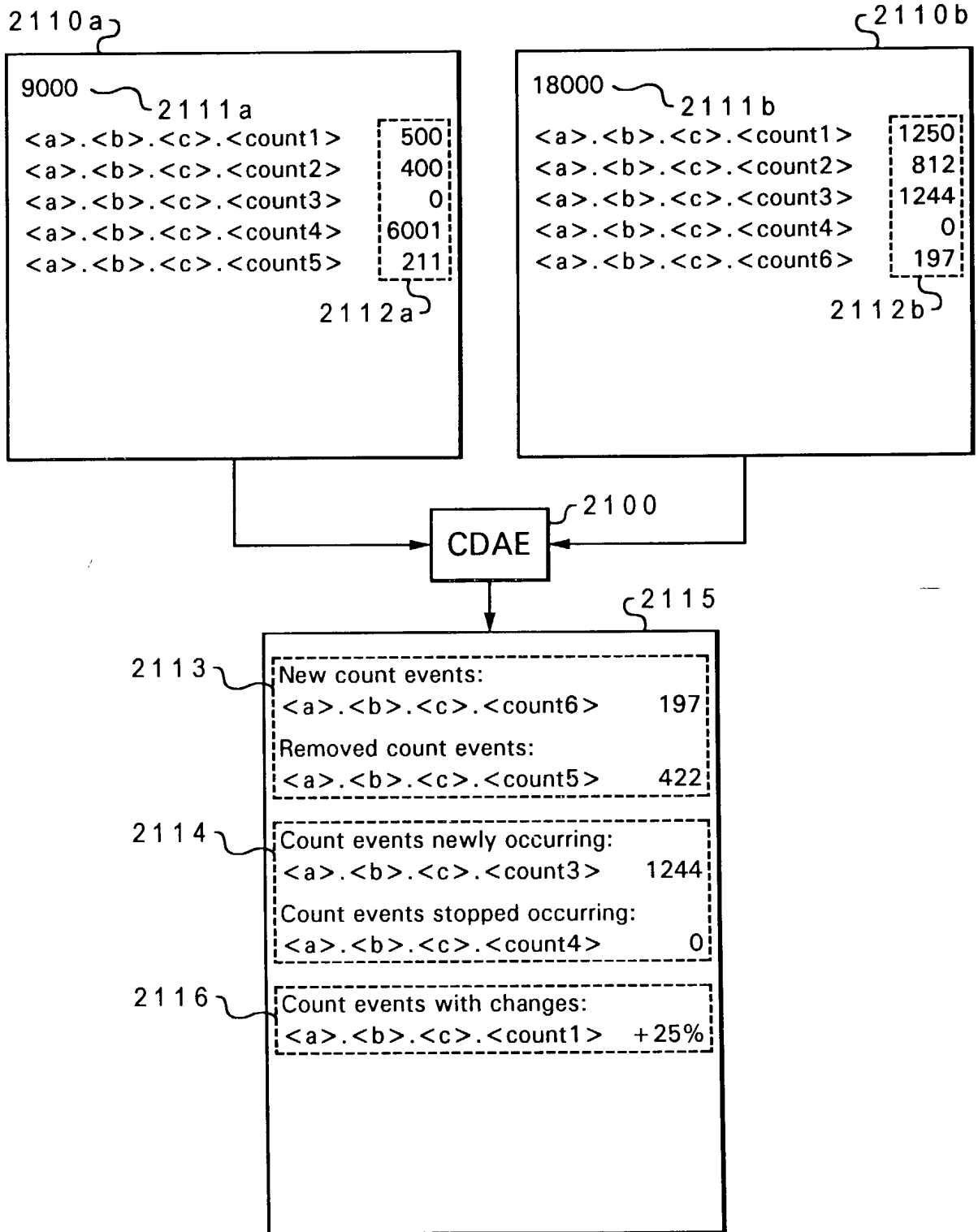


Fig. 21B

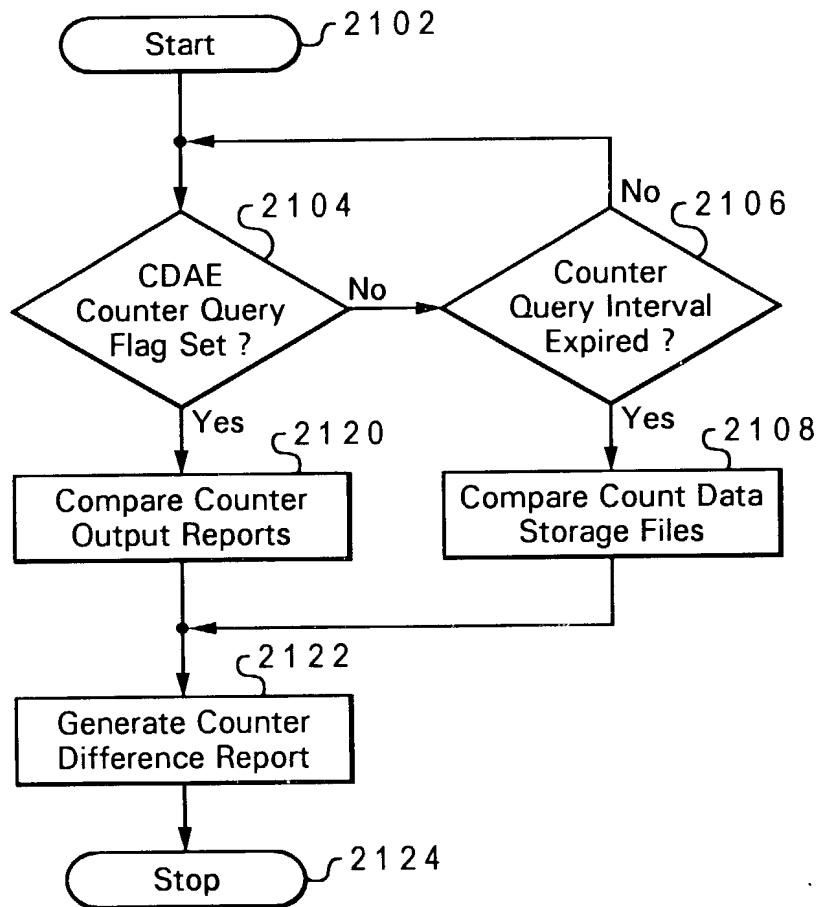
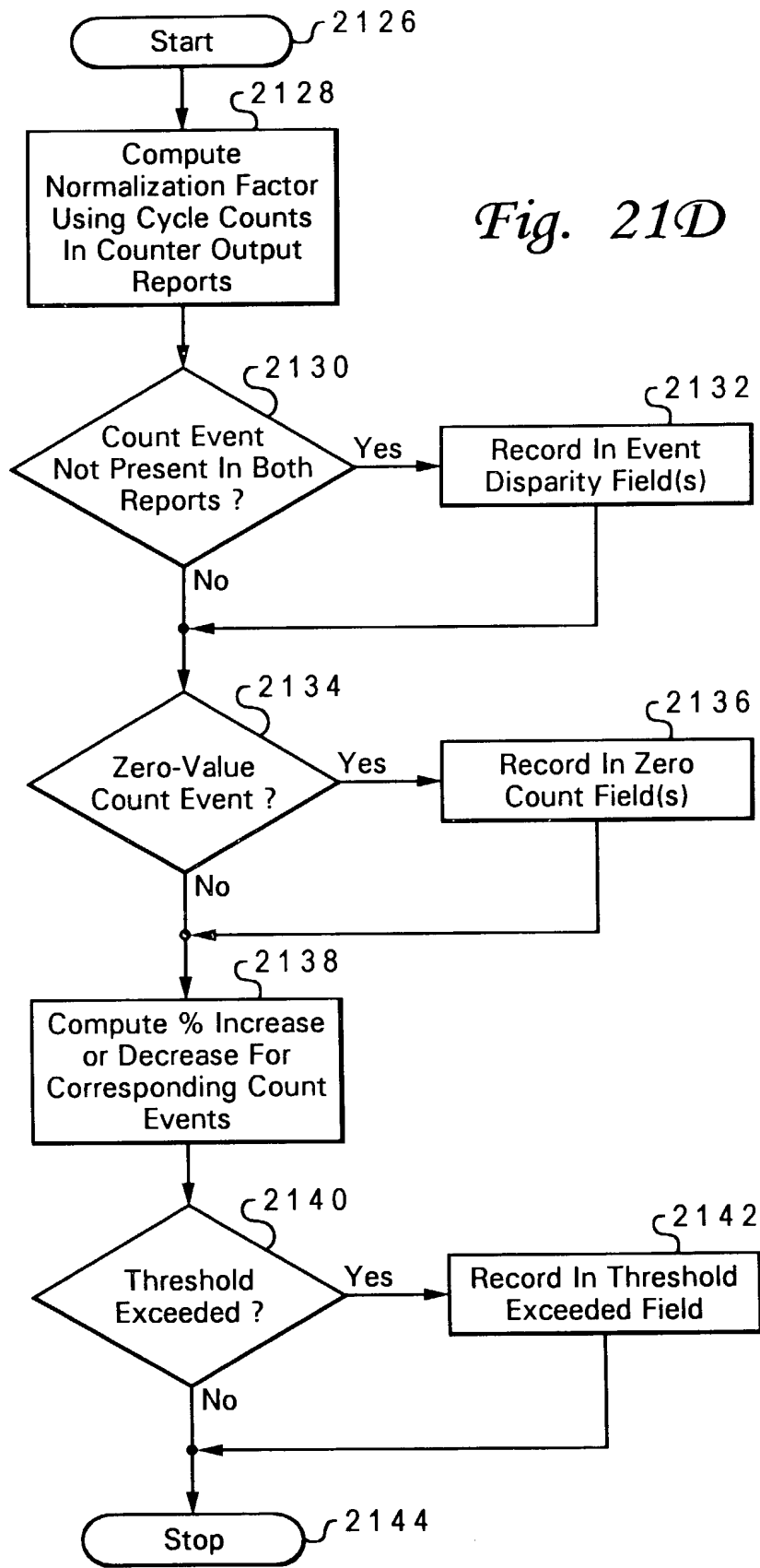


Fig. 21C



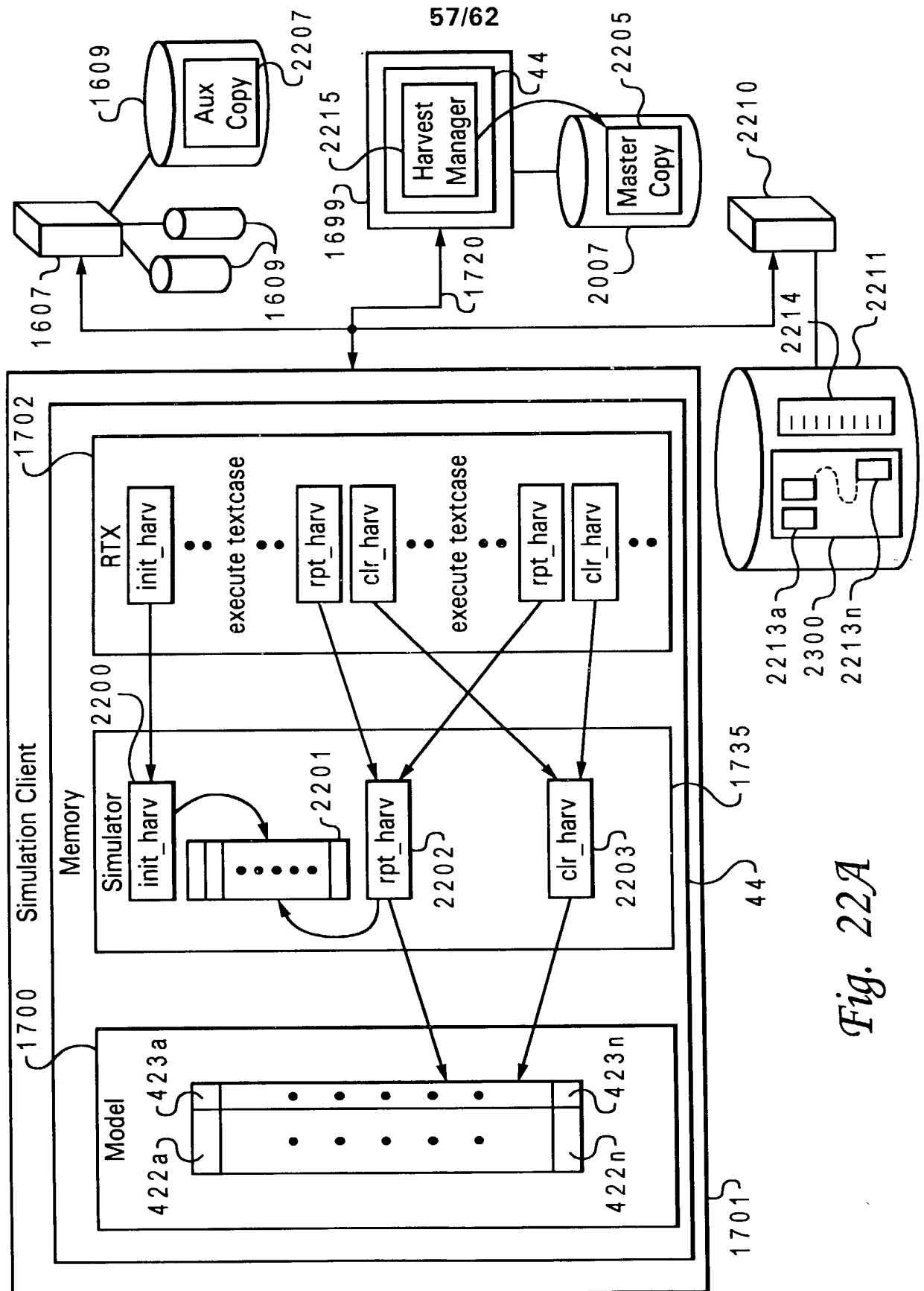


Fig. 22A

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Fig. 22B

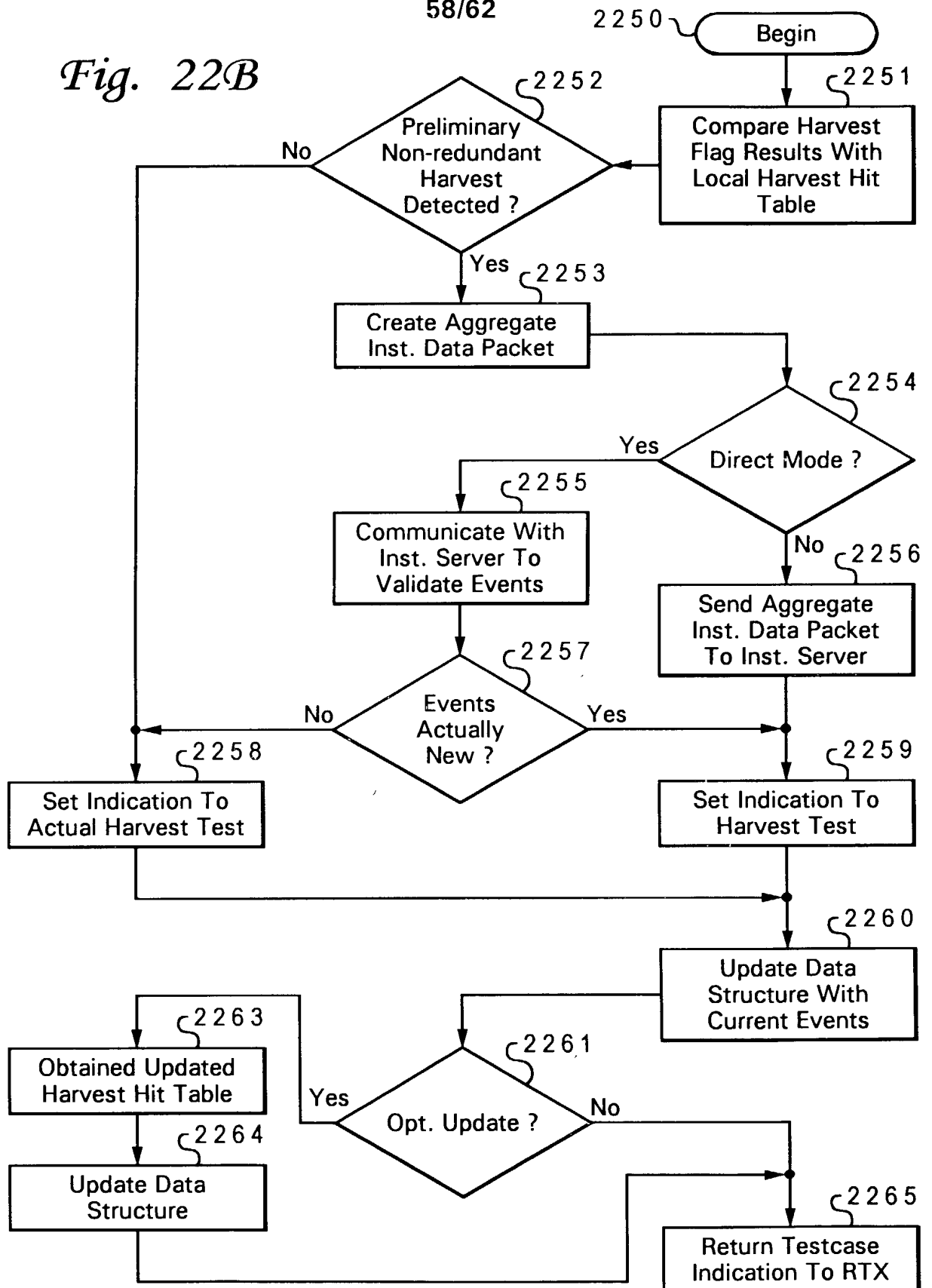
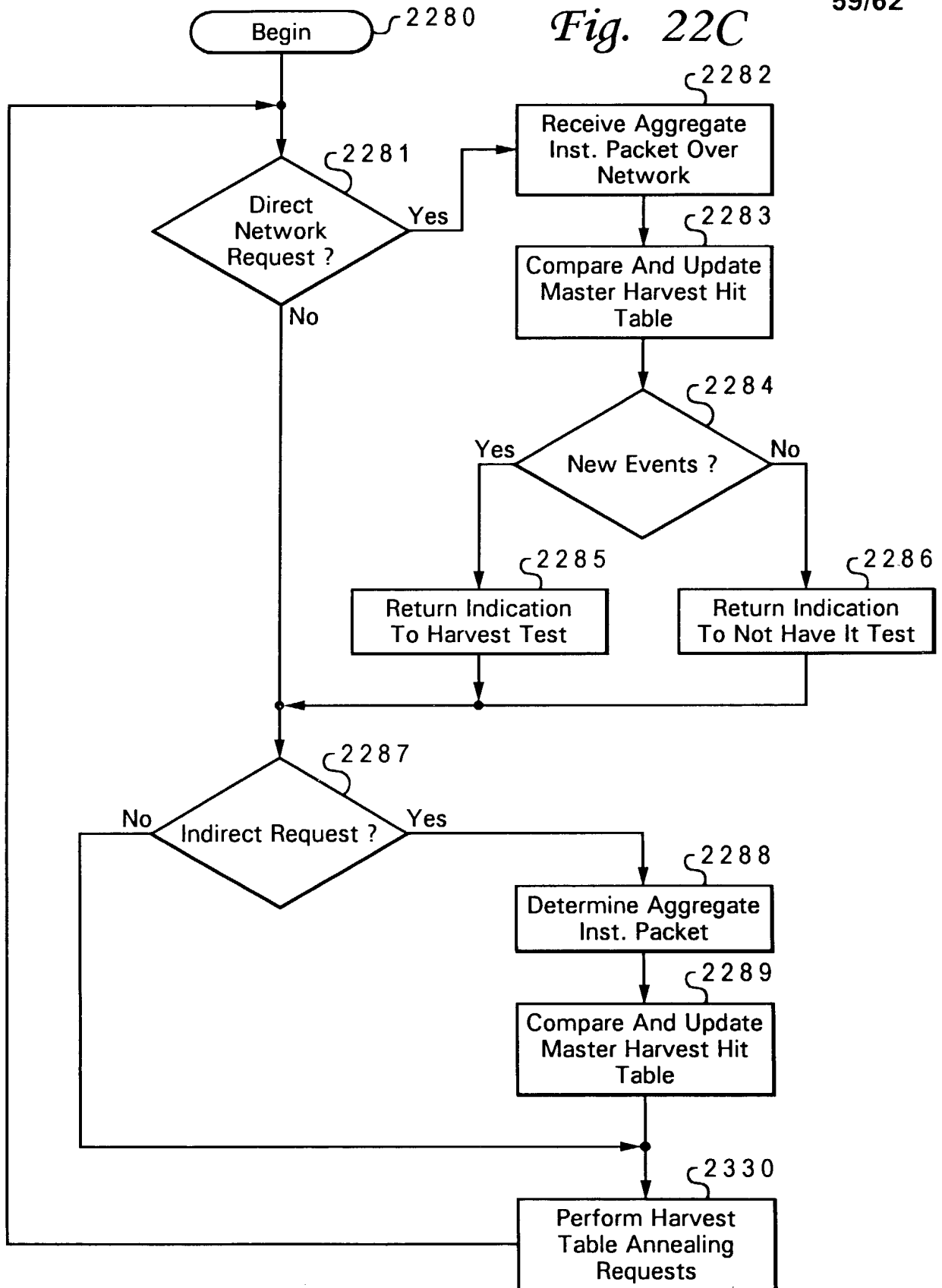


Fig. 22C



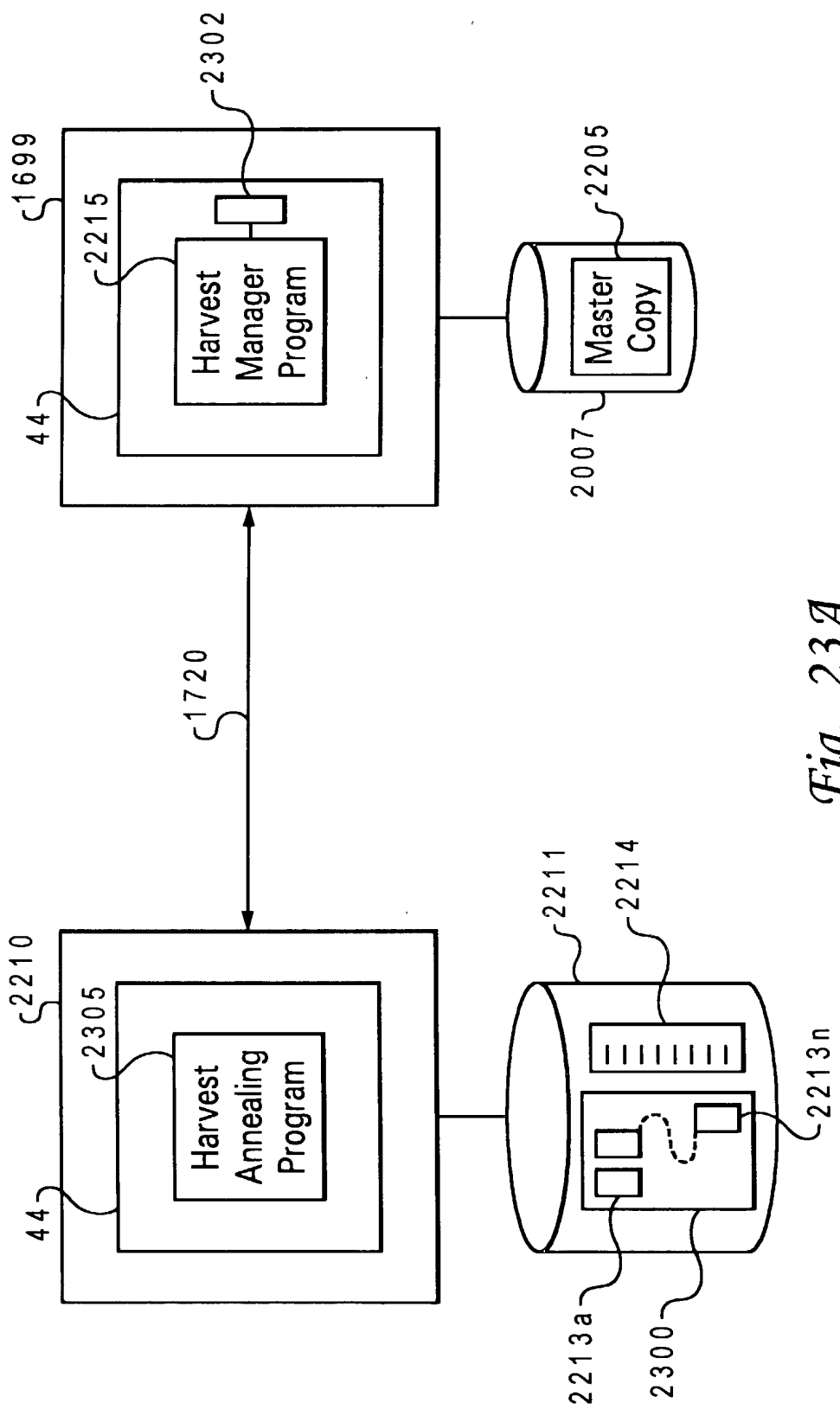


Fig. 23A

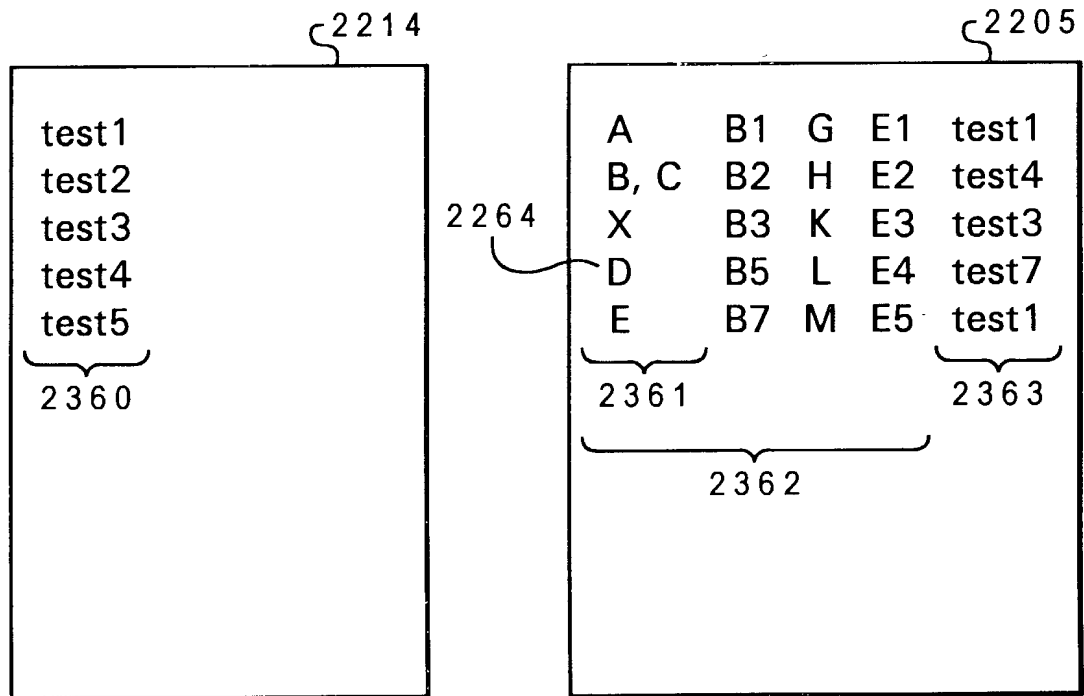


Fig. 23B

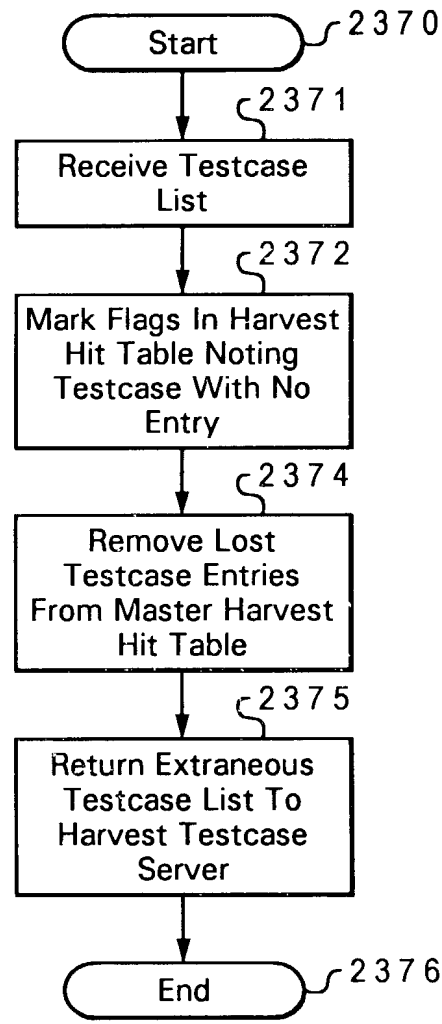


Fig. 23C